تراشه‌های منطقی برنامه پذیر

مرتضی صاحب الزمانی

تراشه‌های منطقی برنامه پذیر

Text Book:

[1] Ulrich Heinkel, et al, “The VHDL Reference: A Practical Guide to Computer-Aided Integrated Circuit Design including VHDL-AMS,” Wiley, 2000.

[2] Clive Maxfield, “The Design Warrior’s Guide to FPGA,” Elsevier, 2004.

[3] Zoran Salcic, Asim Smailagic, “Digital Systems Design and Prototyping Using Field-Programmable Logic and Hardware Description Languages”, 2nd Edition, 2000

References:

Datasheets + References given in the slides

تراشه‌های منطقی برنامه پذیر

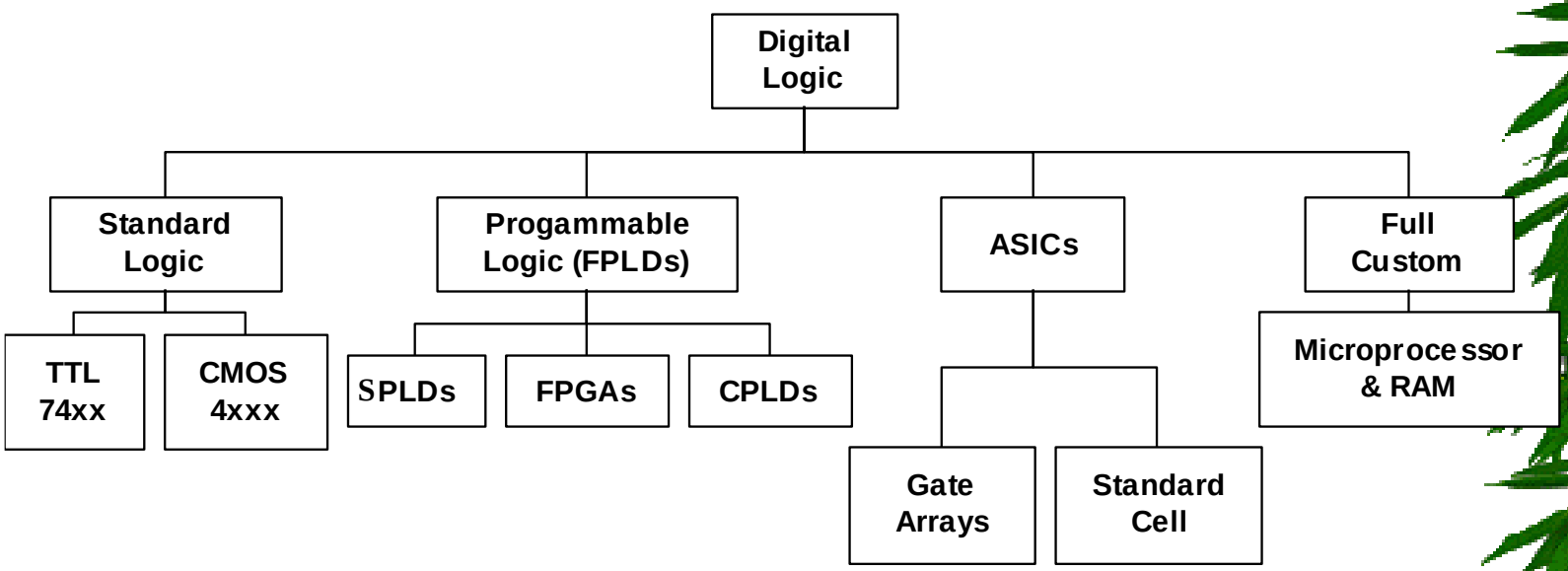
Marking:

Homeworks, Quizes, Project, Midterm Exam, Final Exam.

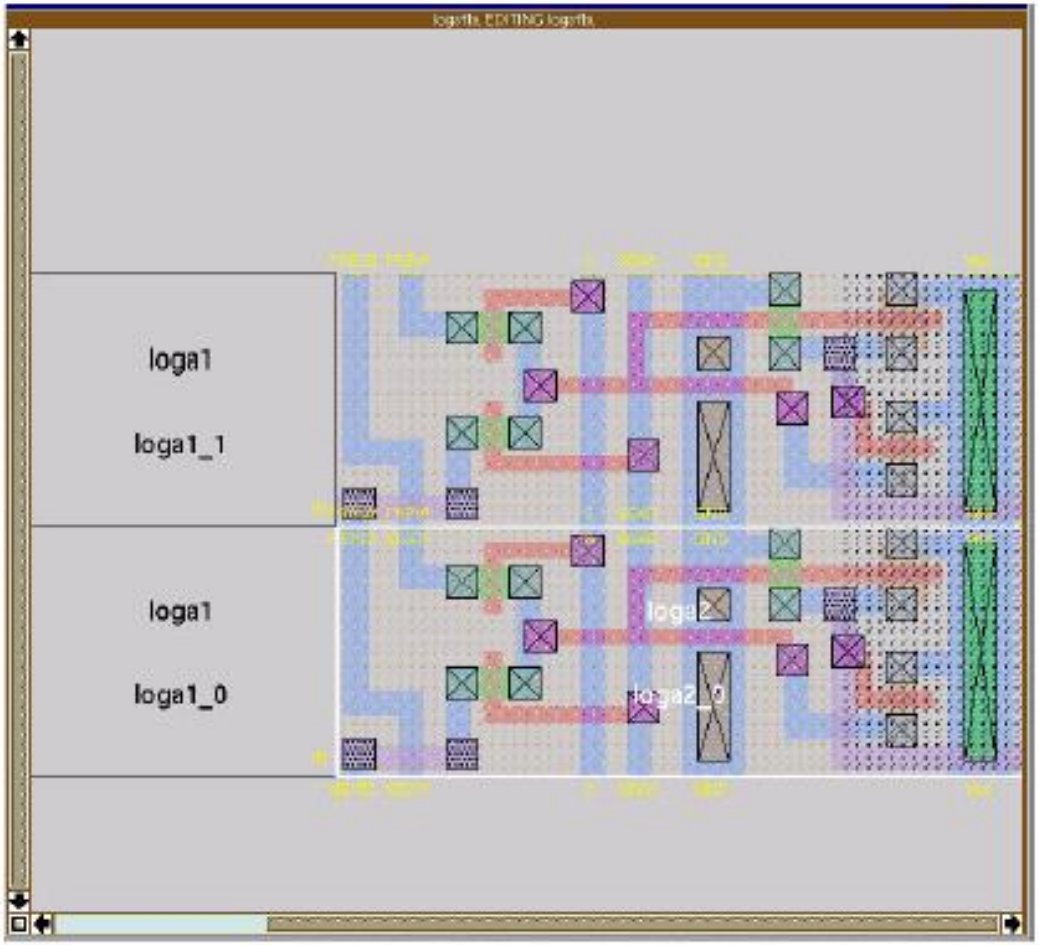
Software:

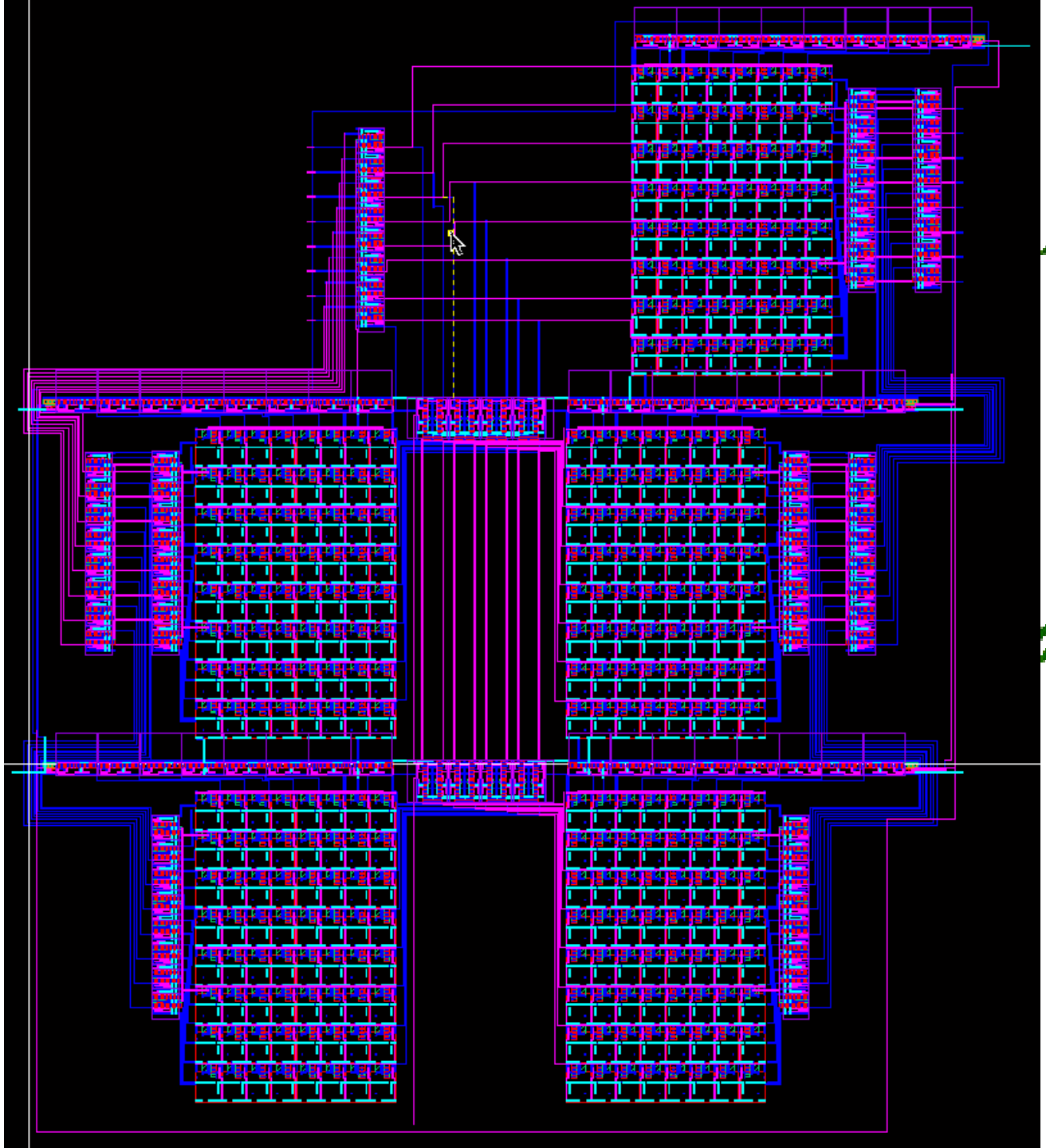
ModelSim, EDK, Quartus

مدارهای دیجیتال



Full-Custom



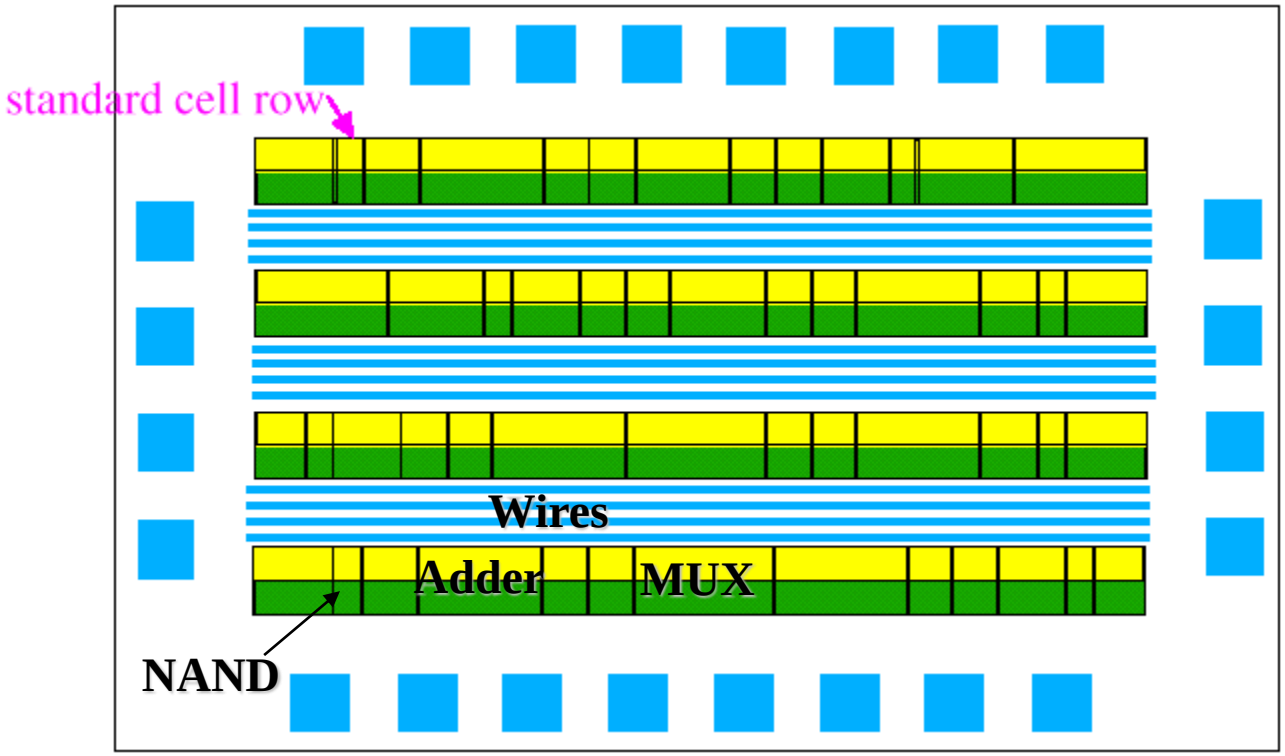


ASIC

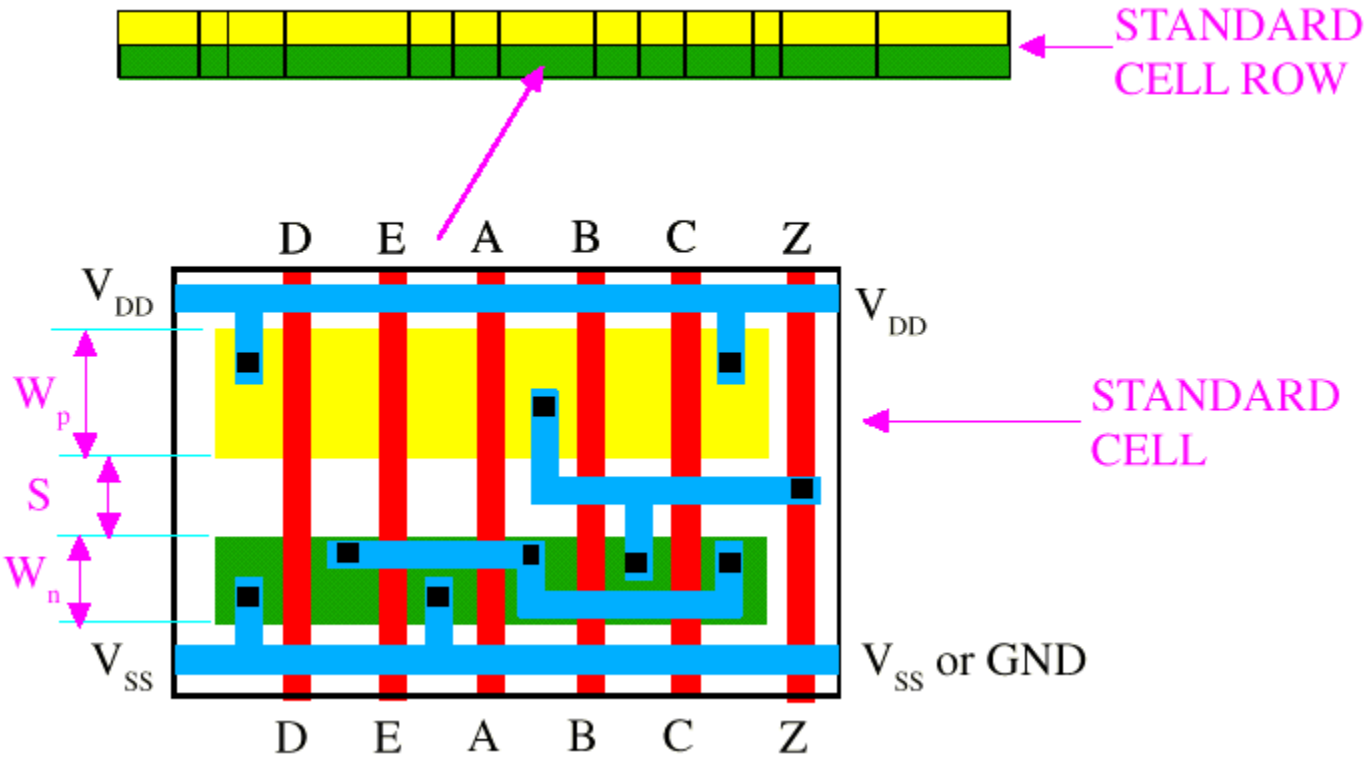
ASIC: Application-Specific Integrated Circuits

- **Standard Cell**: عناصر در ردیفها چیده می شوند. پورتها در بالا و پایین سلولها (تکنولوژی جدید: روی سلولها).
- **Gate Array**: آرایه ای از سلولهای مشابه.

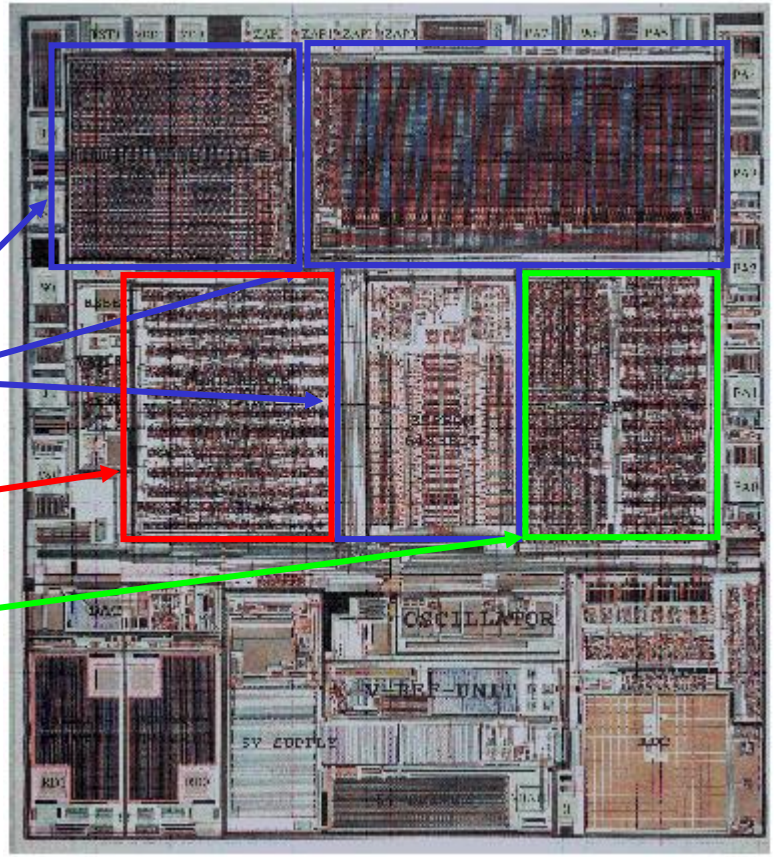
سلولهای استاندارد



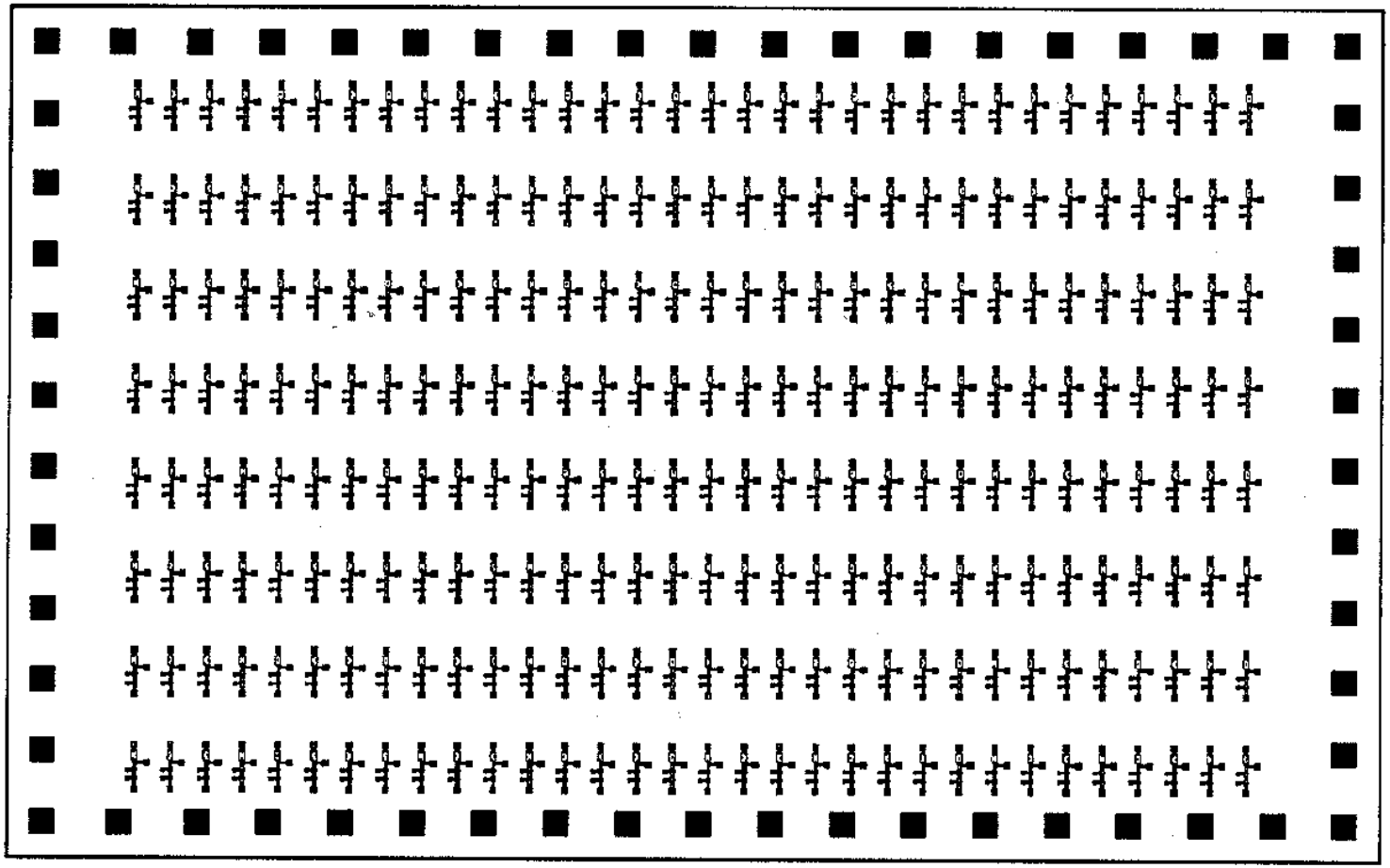
سلولهای استاندارد



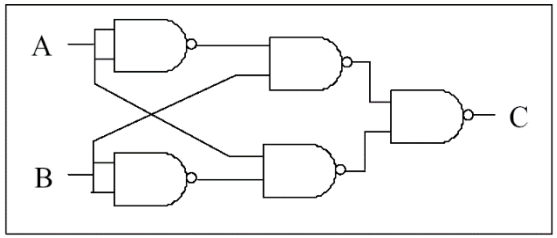
Mixed

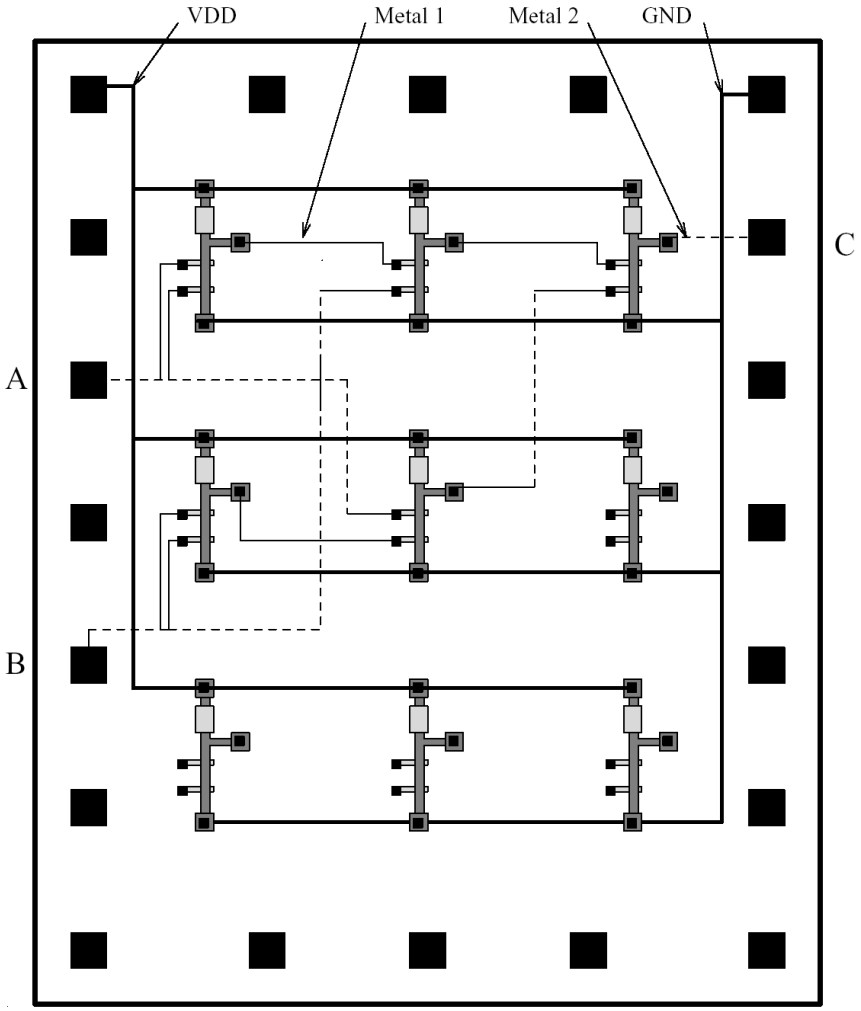


Uncommitted Gate Array



Committed Gate Array





مرتضی صاحب الزمانی

Gate Array

- **MPLD یا MPGA: برنامه ریزی تراشه در زمان ساخت.**
- **FPLD: برنامه ریزی تراشه به صورت الکتریکی توسط کاربر.**

Structured ASIC

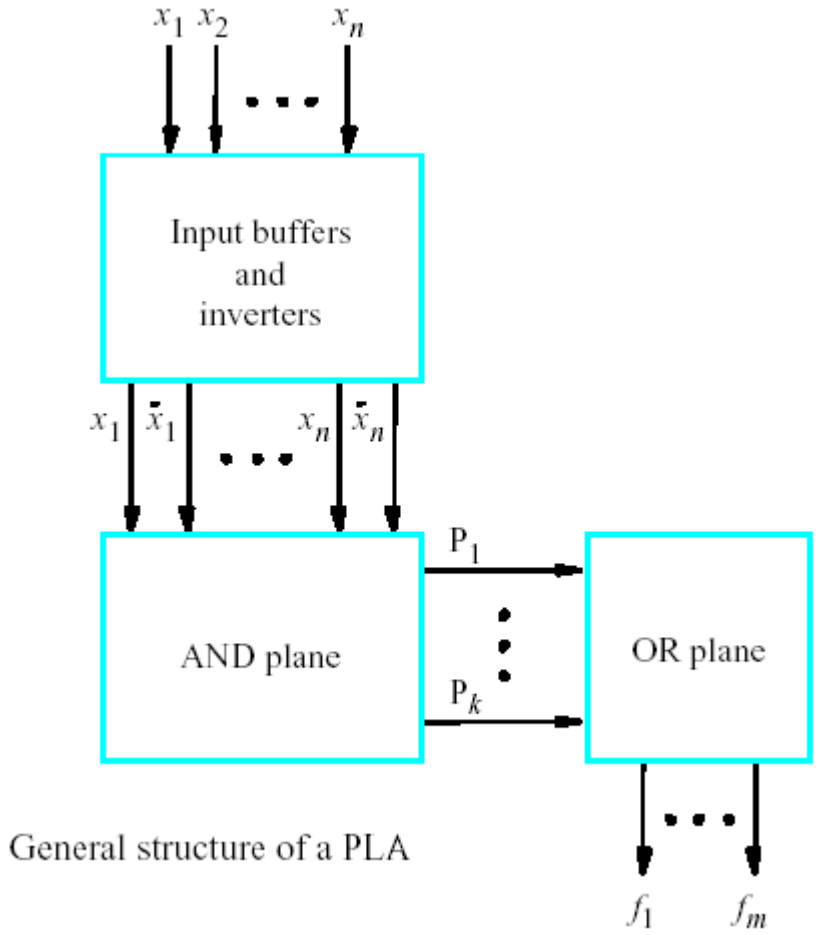
- مانند Gate Array
- تشابه:
  - فقط لایه‌های فلز سفارشی می‌شوند
  - هزینه ساخت ماسک‌ها خیلی کم

Structured ASIC

- مانند Gate Array
- تفاوت:
  - گیت‌های خیلی پیچیده: MUX، LUT
  - بیشتر لایه‌های فلز ساخته شده‌اند
  - هزینه کمتر و سرعت بالاتر و توان مصرفی کمتر

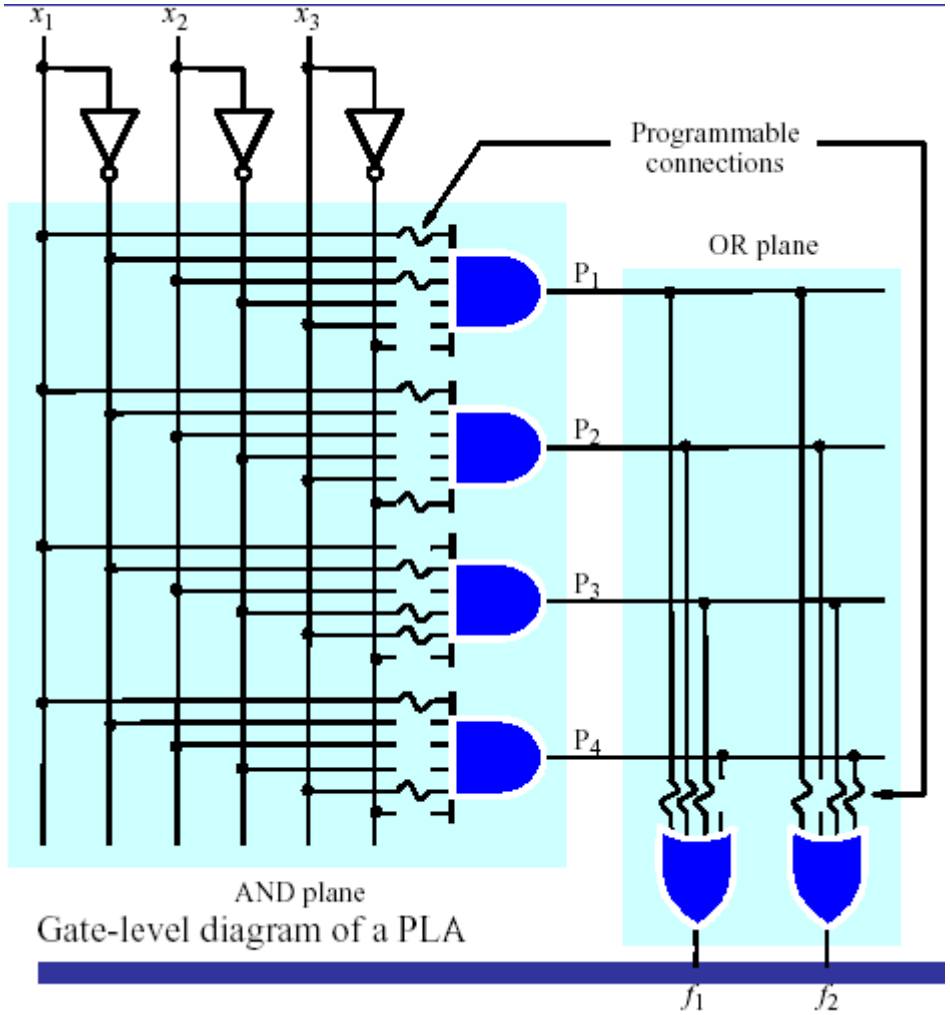
مقایسه

Programmable Logic Array (PLA)



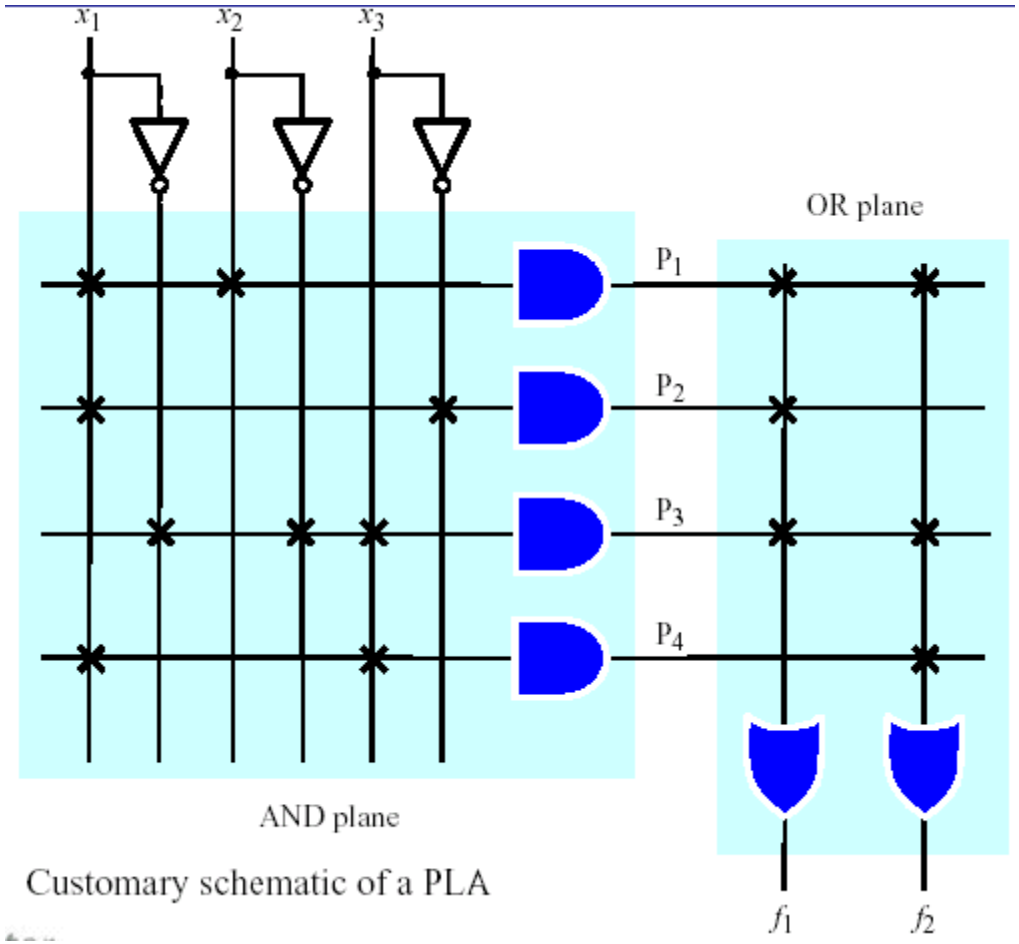
General structure of a PLA

PLA



Gate-level diagram of a PLA

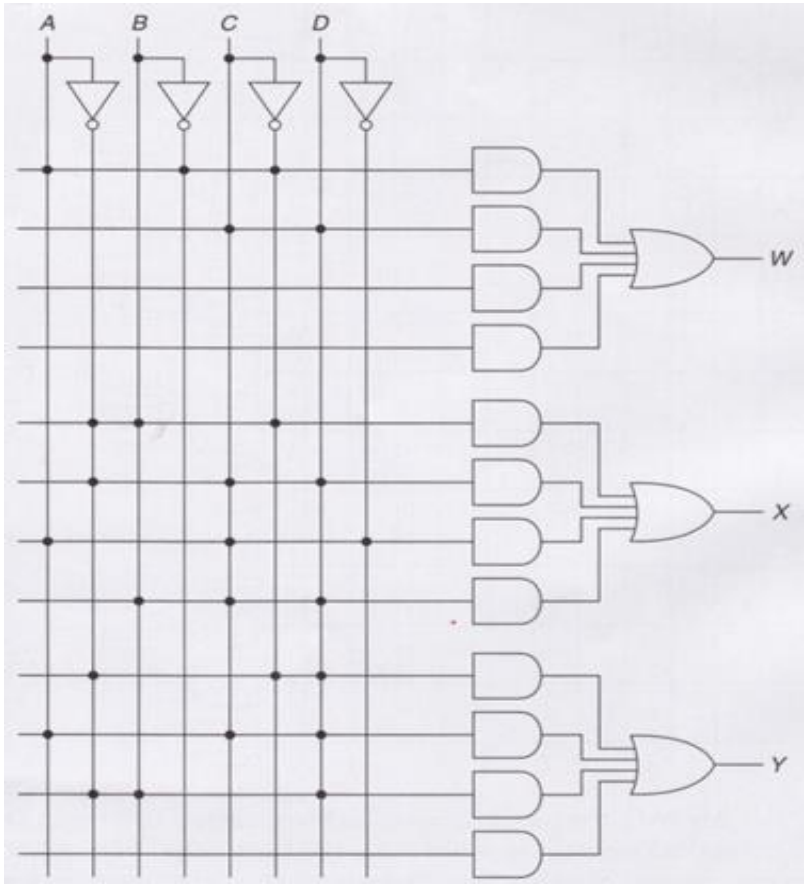
PLA



Customary schematic of a PLA

PAL

- فقط **AND Plane** قابل برنامه ریزی.



$W = AB'C' + CD$

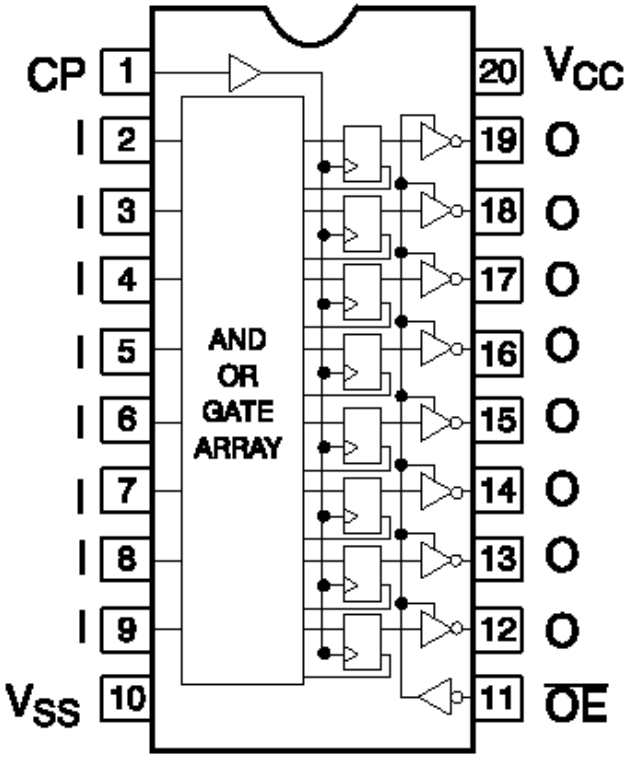
$X = A'BC' + A'CD + ACD' + BCD$

$Y = A'C'D + ACD + A'BD$

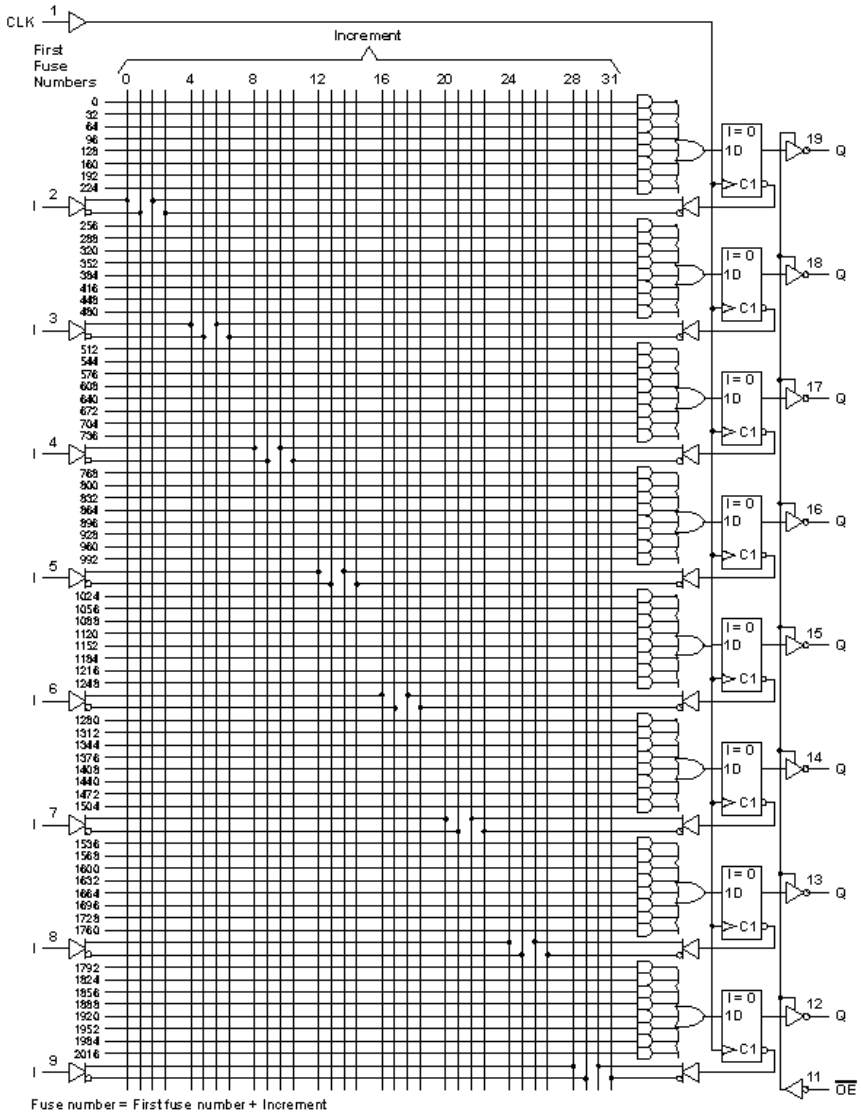
Programmable Array Logic (PAL)

- برای پیاده سازی مدارهای ترتیبی معمولا در خروجی، FF قرار دارد.

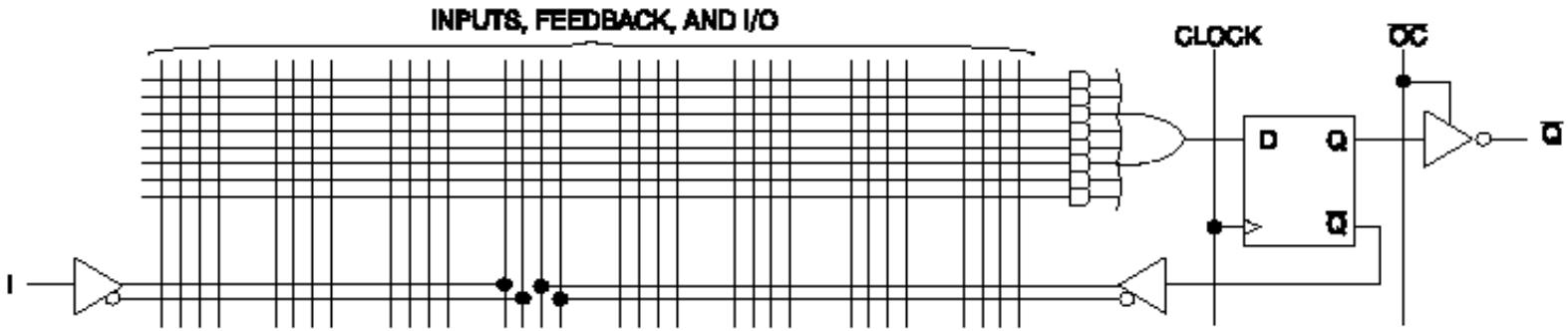
PAL 16R8

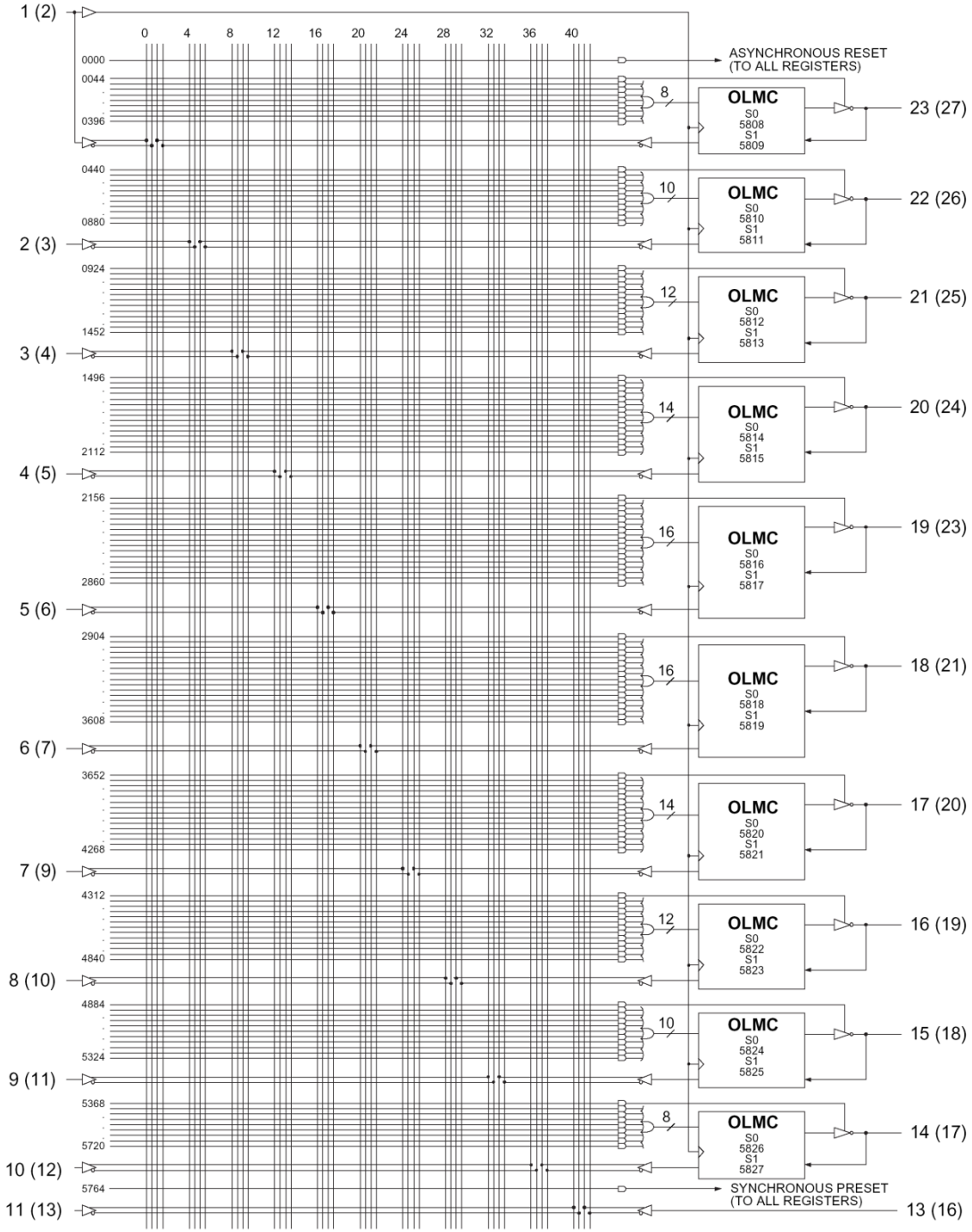


PAL 16R8

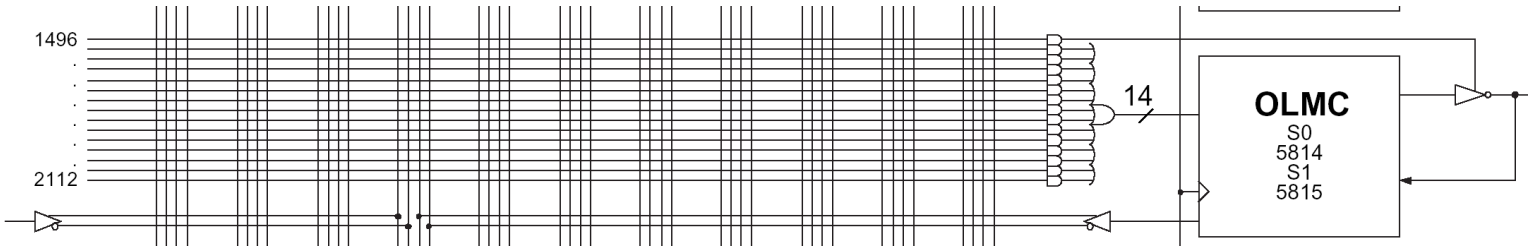

CLK
1
Increment
First
Fuse
Numbers
0
4
8
12
16
20
24
28
31
I
2
3
4
5
6
7
8
9
I = 0
1D
C1
Q
19
18
17
16
15
14
13
12
11
OE
Fuse number = First fuse number + Increment

PAL 16R8

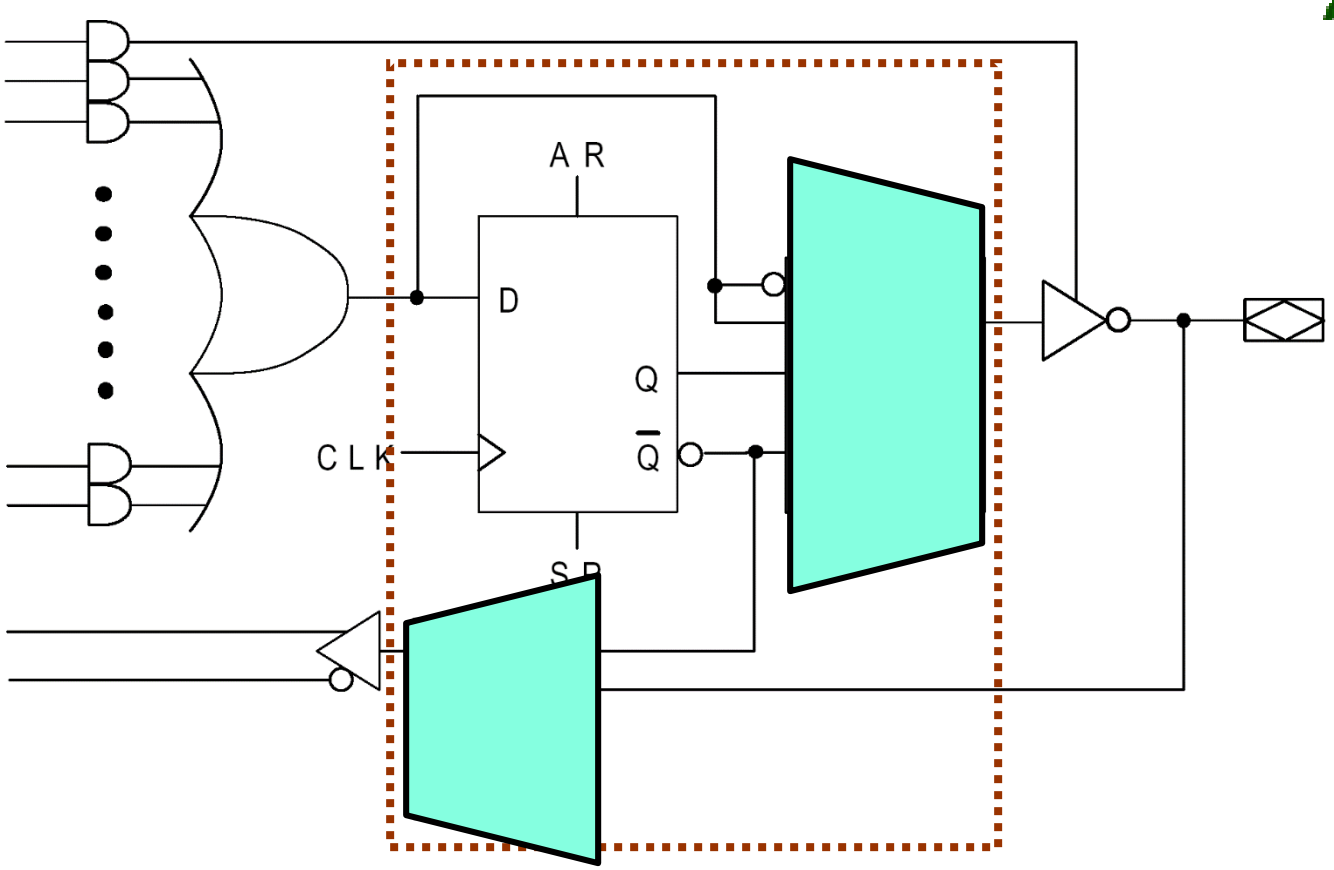



1 (2)
0 4 8 12 16 20 24 28 32 36 40
0000
0044
0396
ASYNCHRONOUS RESET
(TO ALL REGISTERS)
8
OLMC
S0
5808
S1
5809
23 (27)
0440
0880
10
OLMC
S0
5810
S1
5811
22 (26)
2 (3)
0924
1452
12
OLMC
S0
5812
S1
5813
21 (25)
3 (4)
1496
2112
14
OLMC
S0
5814
S1
5815
20 (24)
4 (5)
2156
2860
16
OLMC
S0
5816
S1
5817
19 (23)
5 (6)
2904
3608
16
OLMC
S0
5818
S1
5819
18 (21)
6 (7)
3652
4268
14
OLMC
S0
5820
S1
5821
17 (20)
7 (9)
4312
4840
12
OLMC
S0
5822
S1
5823
16 (19)
8 (10)
4884
5324
10
OLMC
S0
5824
S1
5825
15 (18)
9 (11)
5368
5720
8
OLMC
S0
5826
S1
5827
14 (17)
10 (12)
5764
SYNCHRONOUS PRESET
(TO ALL REGISTERS)
11 (13)
13 (16)

22V10 SPLD

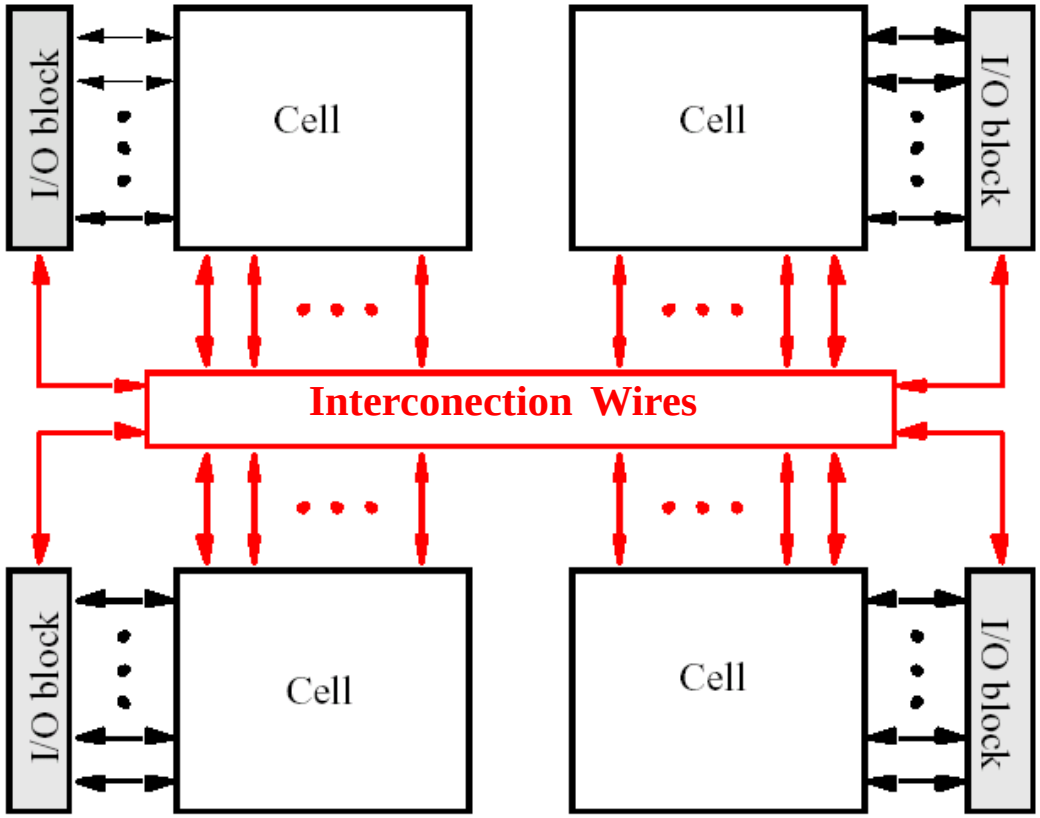


SPLD Macrocell

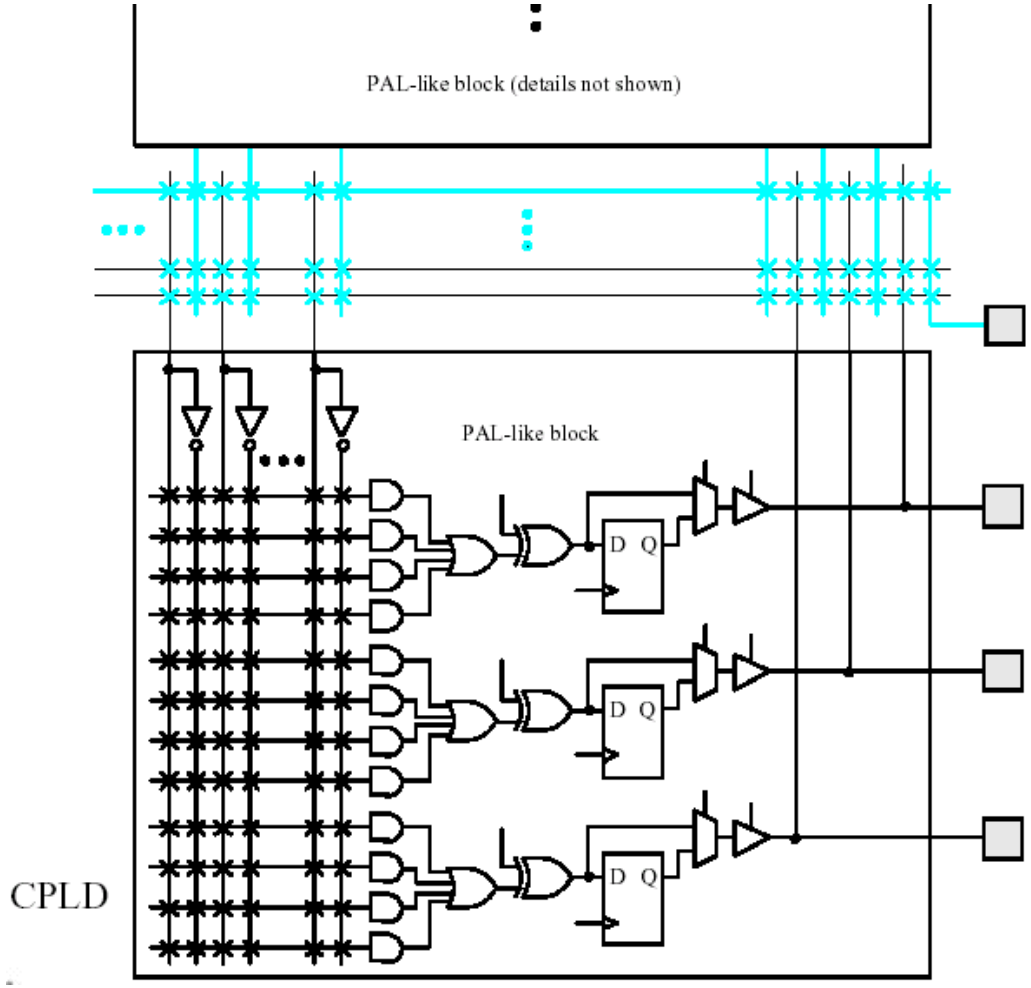


GAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

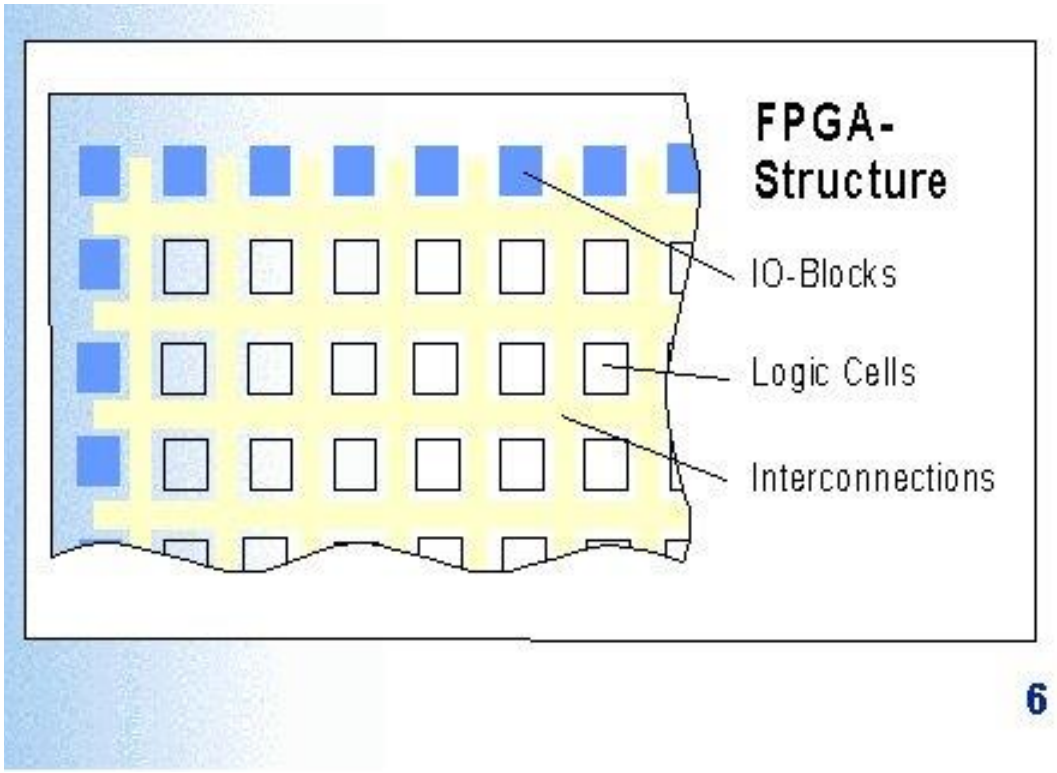
CPLD


I/O block
Cell
Cell
I/O block
Interconection Wires
I/O block
Cell
Cell
I/O block

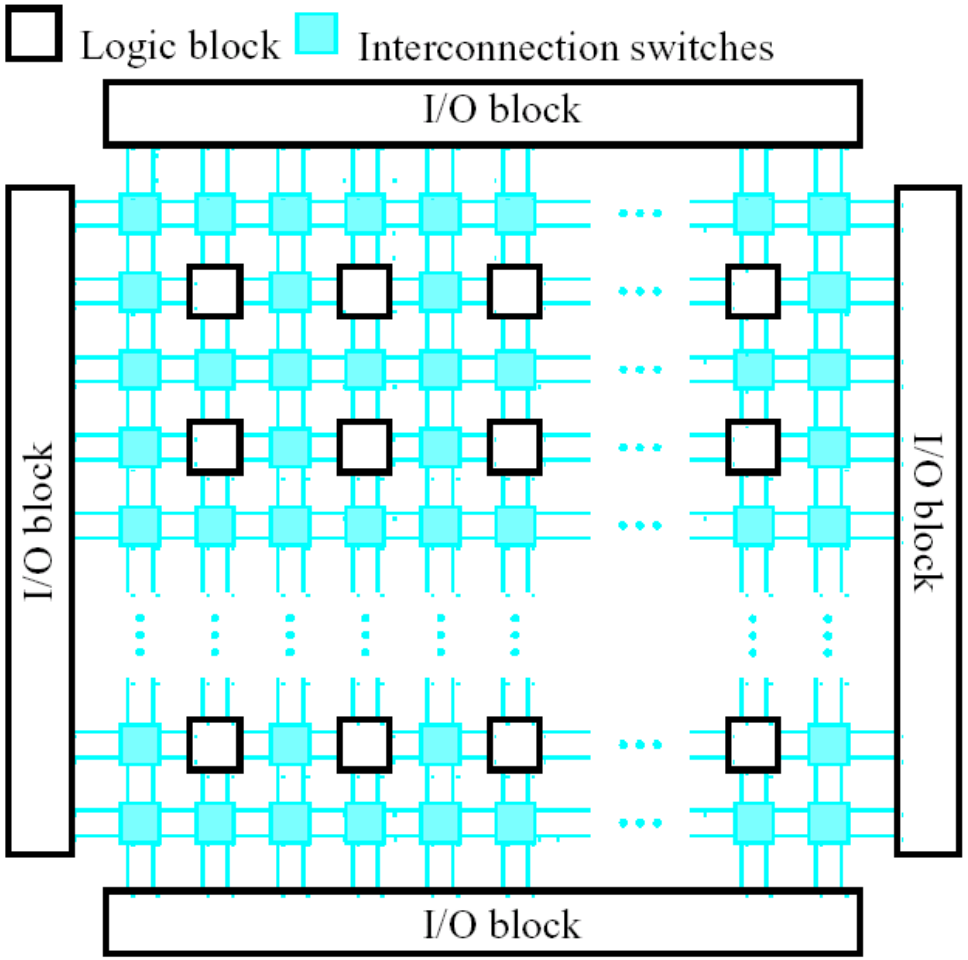
بخشی از CPLD



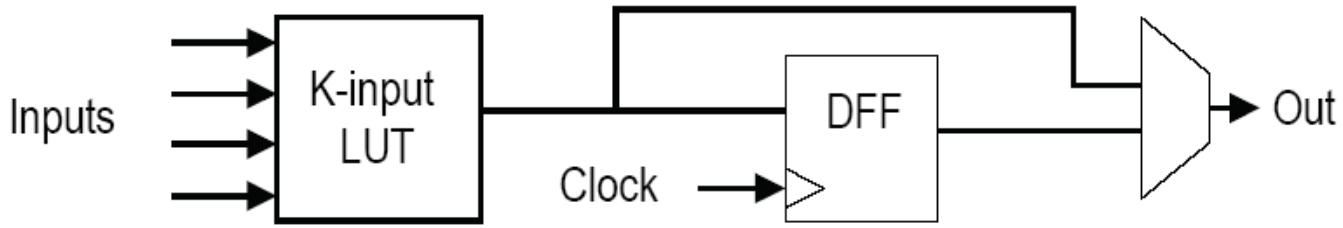
ساختار FPGA



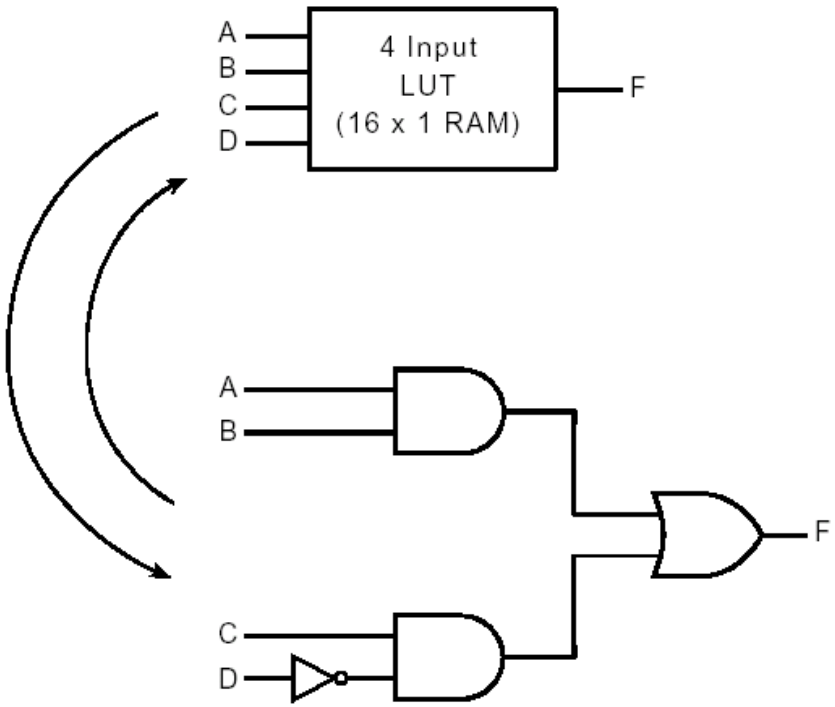
ساختار FPGA


Logic block
Interconnection switches
I/O block
I/O block
I/O block
I/O block

Logic Cell



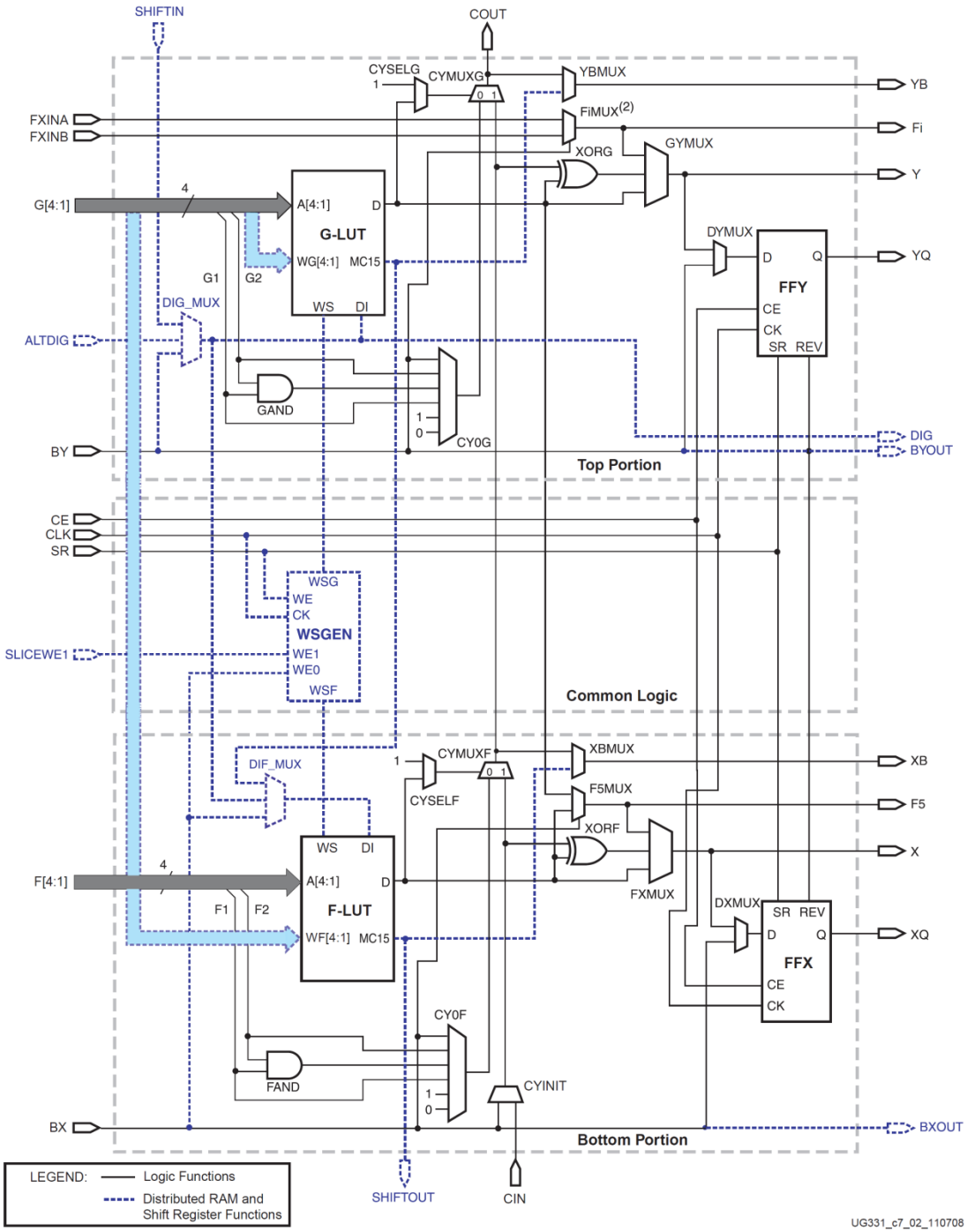
LUT



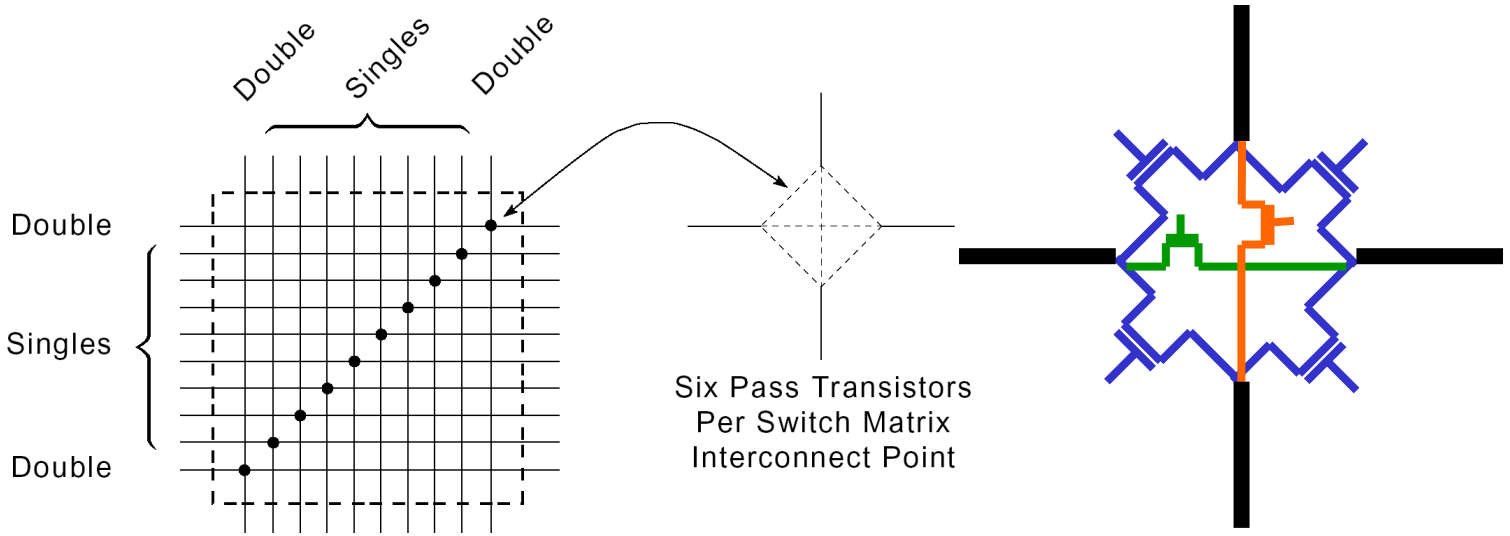
RAM Contents				
Address				Data
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Using a lookup table (LUT) to model a gate network.

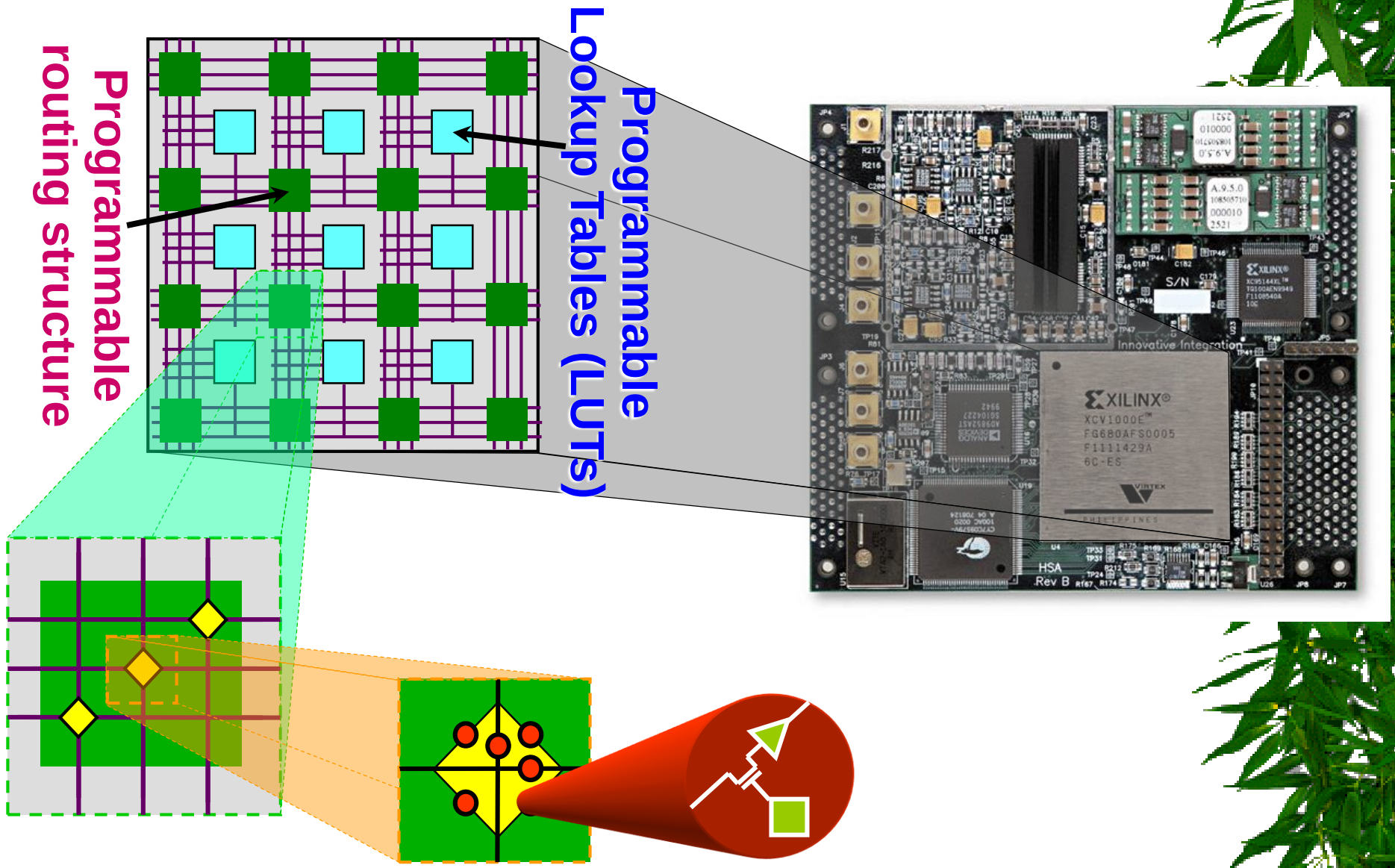
Spartan Logic Cell



Programmable Switch Matrix (PSM)



SRAM-Based FPGA



Hybrid FPGA & ASIC

- **Use reconfigurable fabric to customize an ASIC**
- **Previously: FPGAs have been used to augment ASIC chips in board level**
- **Now, they can be used on a single chip**