CSE112: Computer Organization

Class Test - III, April 11, 2013: FULL MARKS – 25

NAME:

ROLL#:

1. Assume a cache of size 64KB and number of cache lines is 512. If the cache is 4 way set associative and the virtual address is 32 bits then find the number of offset, tag and set bits required.

# of cache line 512, associativity = 4 **(2 Marks)**

# of sets = 512/4 = 128, i.e. index = 7 bits

block size = 64 × 1024 / 512 byte = 128 byte, offset = 7 bit

Tag (assuming VM space = phy mem) = 32 − 14 = 18 bit

2. You find that it would be very inexpensive to implement small, direct mapped cache of 32K bytes with an access time of 30 ns. However, the hit rate would be only about 50%. If the main memory access time is 60 ns, does it make sense to implement the cache? Give a quantitative explanation. **[3 marks]**

Cache access time 30 ns.

Avg. mem access time := cache access time
+ miss rate × penalty

= 30 + .5 × 60 = 60 ns.

No improvement on mem access time despite implementing cache.

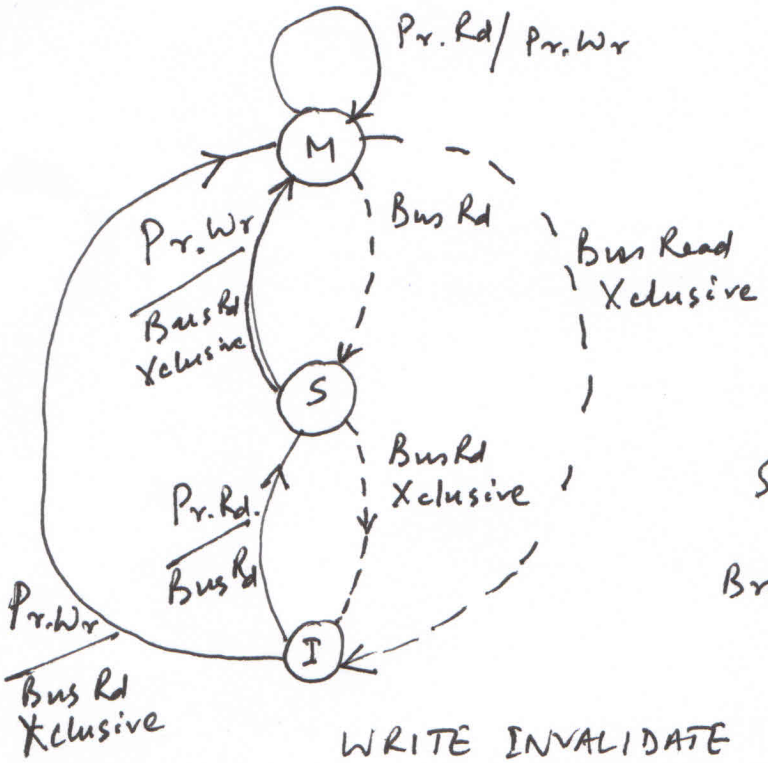
DOESN'T MAKE SENSE TO IMPLEMENT CACHE.

3. (a) Draw the diagram for write invalidate snoopy protocol for cache coherence with only 3 states i.e. Modified, Shared, and Invalid only. Show the state transition diagram for processor initiated and bus initiated read hit and miss, write hit and miss scenarios.

(b) For a write through protocol how many states are required in minimum to keep the cache coherent? Show the state diagram.

(3 + 3 marks)

(a)

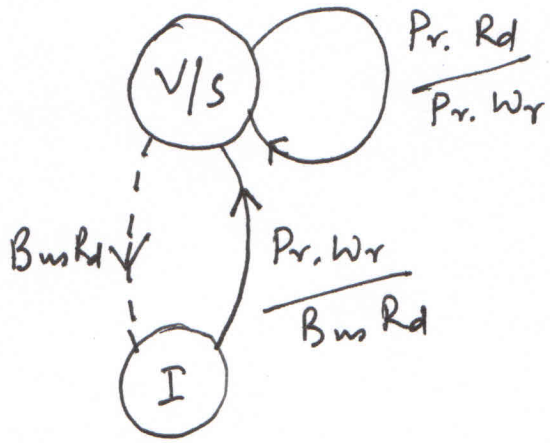


Solid Line = local action

Broken Line = action from other proc./bus.

WRITE INVALIDATE

(b) For write update / through 2 state are sufficient. 1 Invalid state and 1 valid or Shared state



Solid = local action

Broken line = action from other proc. or bus.

4. Assume the following set of instructions. How would the above program change if Branch Delay Slot mechanism is used to handle conditional branching above. **(4 Marks)**

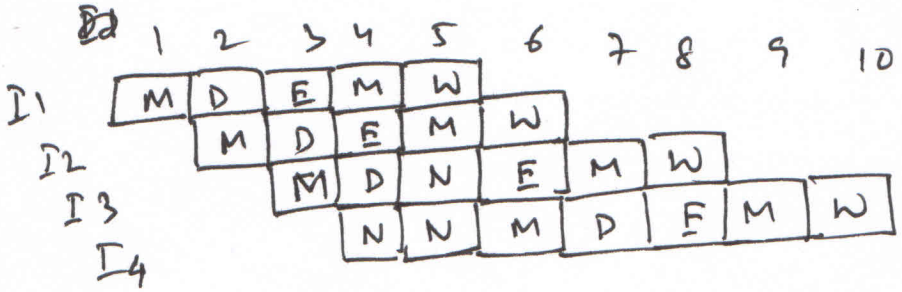
```
LD R1, 20 ($R6);
BNEZ $R1, Label1
ADDI  $R1, $R1, 5

Label 1: LD R2, 60 ($R6);
ADD R3,R1,R2;
ST R3, MEM[2];
```

```
LD  R1, 20 ($R6)
BNEZ  $R1 , Label 1
Label 1 :  LD R2 , 60 ($R6)
ADDI  $R1 , $R1 , 5 [B R. DELAY SLOT]
ADD R3, R1 , R2
ST  R3,  MEM[2].
```

5. Consider the pseudo assembly code for a hypothetical 5 stage pipelined processor with von-Neumann architecture. Write a proper pipeline diagram for the given code. **(5 Marks)**

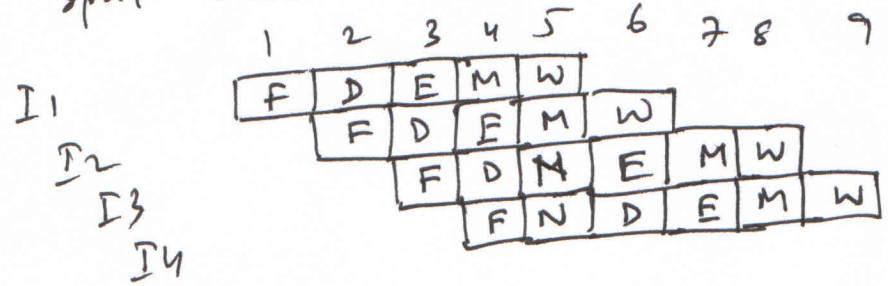
```
LOAD R1, MEM[0];   I1
LOAD R2, MEM[1];   I2
ADD R3,R1,R2;      I3
STORE R3, MEM[2];  I4
```

Assuming Von-Neumann arch. Fetch / Inst Mem = Data mem.



N = NOP bubble.

For split Fetch & Data mem:→



6. Assume that a branch has following outcome in a row: T (Taken), T, T, NT (Not Taken) NT.

(a) What is the accuracy of ALWAYS TAKEN and ALWAYS NOT-TAKEN predictor for this sequence of branch outcome?

(b) What is the accuracy of the two bit predictor if this pattern is repeated forever? You can assume that the predictor start from STRONGLY NOT TAKEN (00) state. **(2+3)**

(a) Always taken

2 NT outcome

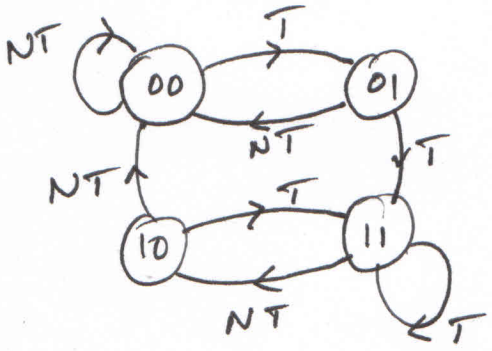
accuracy = $\frac{3}{5}$ = 60 %

Always NT

2 T outcome

accuracy = $\frac{2}{5}$ = 40 %

(b) Assuming a state transition diagram where two misprediction from a Strongly T taken to Strongly NT



	From State	Prediction	Outcome	To state
1st Iteration	00	NT	T	01
	01	NT	T	11
	11	T	T	11
	11	T	NT	10
	10	T	NT	00
2nd Iteration	00	⋮	→ Repeats itself.	
	01	⋮		

1 correct prediction ⇐

accuracy = $\frac{1}{5}$ = 20 %.

Assuming sequential counts → 00 → 01 → 10 → 11

State	Pred.	Outcome	to state
00	NT	T	01
01	NT	T	10
10	T	T	11
11	T	NT	10
10	T	NT	01
01	NT	T	10
10	T	T	11
11	T	T	11
11	T	NT	10
10	T	NT	01 ⇒ Repeats

Accuracy $\frac{2}{5}$ = 40 %