FEATURES

- Low voltage and low power operations:
  - FT24C02/04/08/16: V_{CC} = 2.5V to 5.5V
  - FT24C02A/04A/08A/16A: V_{CC} = 1.8V to 5.5V
- Maximum Standby current < 1µA (typically 0.02µA and 0.06µA @ 1.8V and 5.5V respectively).
- 16 bytes page write mode.
- Partial page write operation allowed.
- Internally organized: 256 × 8 (2K), 512 × 8 (4K), 1024 × 8 (8K), 2048 × 8 (16K).
- Standard 2-wire bi-directional serial interface.
- Schmitt trigger, filtered inputs for noise protection.
- Self-timed programming cycle (5ms maximum).
- Automatic erase before write operation.
- Write protect pin for hardware data protection.
- High reliability: typically 800,000 cycles endurance.
- 100 years data retention.
- Industrial temperature range (-40° C to 85° C).
- Standard 8-pin PDIP/SOIC/TSSOP Pb-free packages.

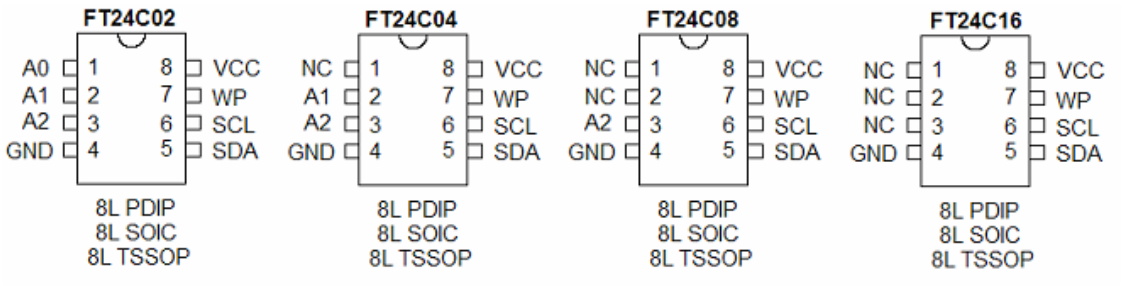
DESCRIPTION

The FT24C02/04/08/16 series are 2048/4096/8192/16384 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM. They are organized as 256/512/1024/2048 words of 8 bits (1 byte) each. The devices are fabricated with proprietary advanced CMOS process for low power and low voltage applications. These devices are available in standard 8-lead PDIP, 8-lead JEDEC SOIC and 8-lead TSSOP packages. A standard 2-wire serial interface is used to address all read and write functions. Our extended V_{CC} range (1.8V to 5.5V) devices enables wide spectrum of applications.

PIN CONFIGURATION

Pin Name	Pin Function
A2, A1, A0	Device Address Inputs
SDA	Serial Data Input / Open Drain Output
SCL	Serial Clock Input
WP	Write Protect
NC	No-Connect

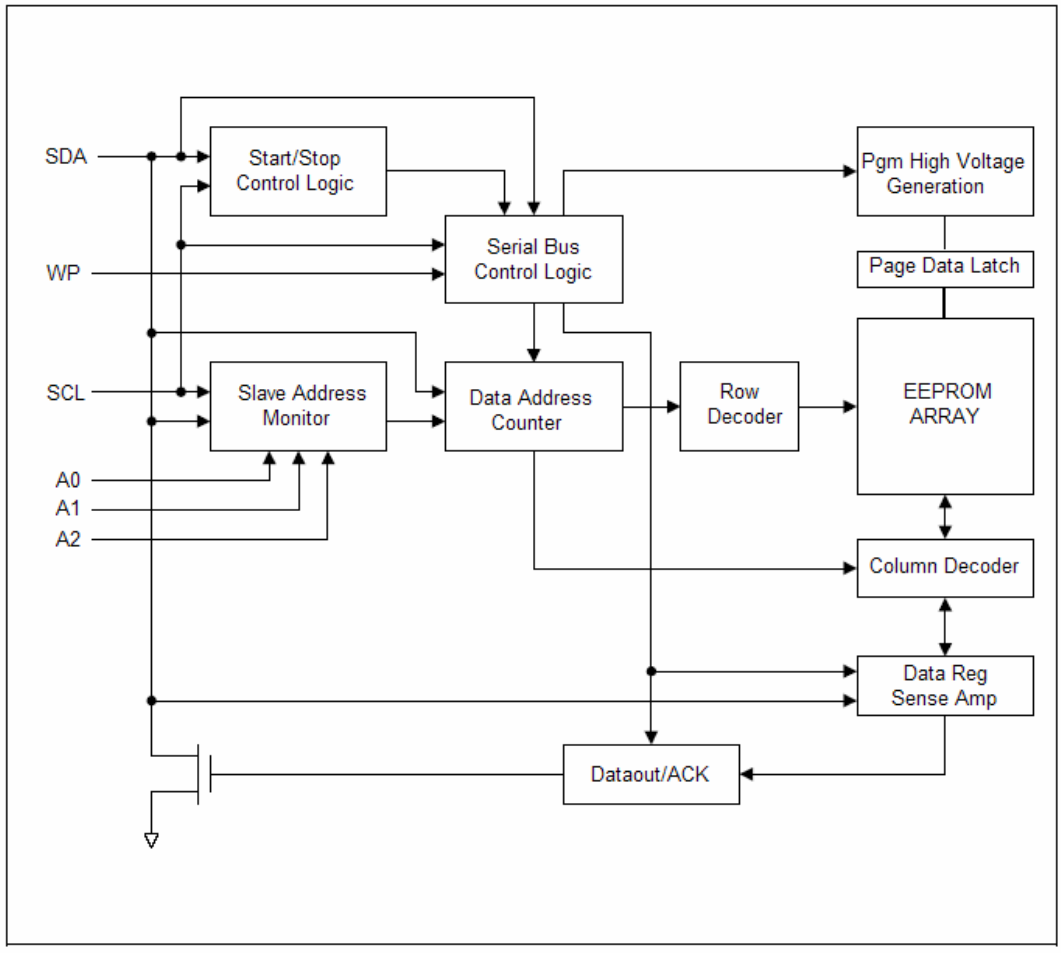
All three packaging types come in conventional or Pb-free certified.



ABSOLUTE MAXIMUM RATINGS

Industrial operating temperature:	-40°C to 85°C
Storage temperature:	-50°C to 125°C
Input voltage on any pin relative to ground:	-0.3V to V_{CC} + 0.3V
Maximum voltage:	8V

** Stresses exceed those listed under "Absolute Maximum Rating" may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality.*



Block Diagram

PIN DESCRIPTIONS

(A) SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the falling edge of this clock is to clock data out of the EEPROM device.

(B) DEVICE / CHIP SELECT ADDRESSES (A2, A1, A0)

These are the chip select input signals for the serial EEPROM devices. Typically, these signals are hardwired to either V_{IH} or V_{IL}. If left unconnected, they are internally recognized as V_{IL}. Only FT24C02 uses all three signals. FT24C04 has A0 pin as no-connect. FT24C08 has both A0 and A1 pins as no-connect. For FT24C16, all device address pins (A0-A2) are no-connect.

(C) SERIAL DATA LINE (SDA)

SDA data line is a bi-directional signal for the serial devices. It is an open drain output signal and can be wired-OR with other open-drain output devices.

(D) WRITE PROTECT (WP)

The FT24C02/04/08/16 devices have a WP pin to protect the whole EEPROM array from programming. Programming operations are allowed if WP pin is left un-connected or input to V_{IL}. Conversely all programming functions are disabled if WP pin is connected to V_{IH} or V_{CC}. Read operations is not affected by the WP pin's input level.

Table A

Device	Chip Select/Device Address Pins Used	No-Connect Pins	Max number of similar devices on the same bus
FT24C02	A2, A1, A0	(None)	8
FT24C04	A2, A1	A0	4
FT24C08	A2,	A1, A0	2
FT24C16	(None)	A2, A1, A0	1

MEMORY ORGANIZATION

The FT24C02/04/08/16 devices have 16/32/64/128 pages respectively. Since each page has 16 bytes, random word addressing to FT24C02/04/08/16 will require 8/9/10/11 bits data word addresses respectively.

DEVICE OPERATION

(A) SERIAL CLOCK AND DATA TRANSITIONS

The SDA pin is typically pulled to high by an external resistor. Data is allowed to change only when Serial clock SCL is at V_{IL}. Any SDA signal transition may interpret as either a START or STOP condition as described below.

(B) START CONDITION

With SCL $\geq V_{IH}$, a SDA transition from high to low is interpreted as a START condition. All valid commands must begin with a START condition.

(C) STOP CONDITION

With SCL $\geq V_{IH}$, a SDA transition from low to high is interpreted as a STOP condition. All valid read or write commands end with a STOP condition. The device goes into the STANDBY mode if it is after a read command. A STOP condition after page or byte write command will trigger the chip into the STANDBY mode after the self-timed internal programming finish.

(D) ACKNOWLEDGE

The 2-wire protocol transmits address and data to and from the EEPROM in 8 bit words. The EEPROM acknowledges the data or address by outputting a "0" after receiving each word. The ACKNOWLEDGE signal occurs on the 9th serial clock after each word.

(E) STANDBY MODE

The EEPROM goes into low power STANDBY mode after a fresh power up, after receiving a STOP bit in read mode, or after completing a self-time internal programming operation.

Figure 1: Timing diagram for START and STOP conditions

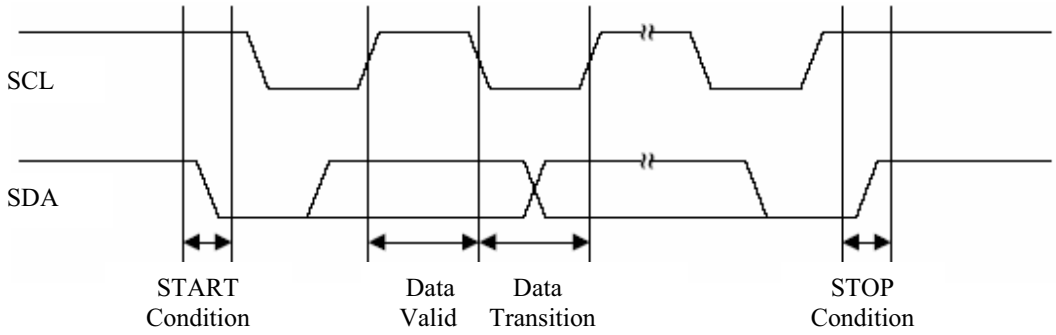
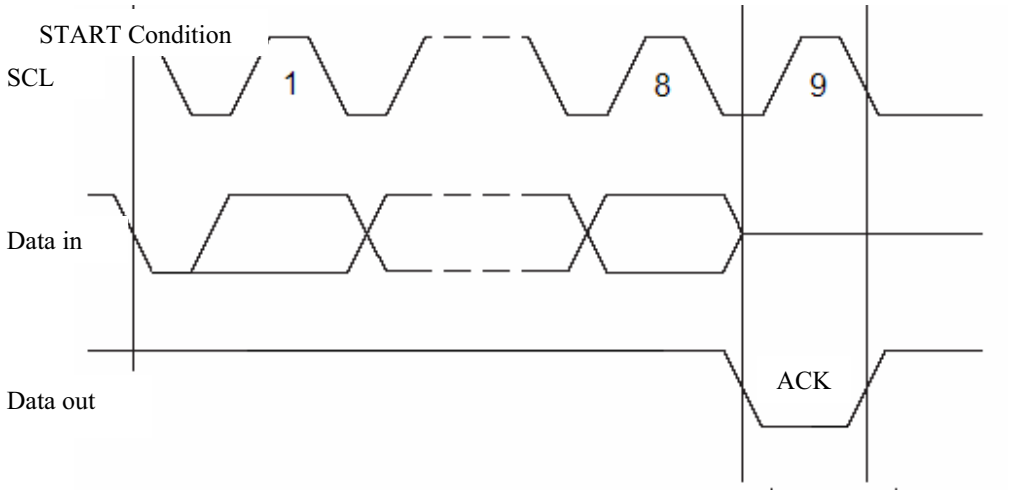


Figure 2: Timing diagram for output ACKNOWLEDGE



DEVICE ADDRESSING

The 2-wire serial bus protocol mandates an 8 bits device address word after a START bit condition to invoke valid read or write command. The first four most significant bits of the device address must be 1010, which is common to all serial EEPROM devices. The next three bits are device address bits. These

three device address bits (5th, 6th and 7th) are to match with the external chip select/address pin states. If a match is made, the EEPROM device outputs an ACKNOWLEDGE signal after the 8th read/write bit, otherwise the chip will go into STANDBY mode. However, matching may not be needed for some or all device address bits (5th, 6th and 7th) as noted below. The last or 8th bit is a read/write command bit. If the 8th bit is at V_{IH} then the chip goes into read mode. If a "0" is detected, the device enters programming mode.

Referring to table A, FT24C02 uses A2 (5th), A1 (6th), and A0 (7th) as device address bits. Up to eight FT24C02 devices can be wired-OR on the same 2-wire bus. Each FT2C02 Chip select address pin needs to be hard wired and coded from 000 (b) to 111 (b). Individual FT24C02 device will be selected if the three device address bits (5th, 6th, 7th) match the chip select address code.

FT24C04 uses A2 (5th) and A1 (6th) device address bits. Only four FT24C04 devices can be wired-OR on the same 2-wire bus. Their corresponding chip select address pins A2 and A1 must be hard wired and coded from 00 (b) to 11 (b). Chip select address pin A0 is not used.

FT24C08 uses only A2 (5th) device address bit. Only two FT24C08 devices can be wired-OR on the same 2-wire bus. Their corresponding chip select address pin A2 must be hard-wired and coded from 0 (b) to 1 (b). Chip select address pins A1 and A0 are not used.

FT24C16 does not use any device address bit. Only one FT24C16 device can be used on the on 2-wire bus. Chip Select address pins A2, A1, and A0 are not used.

WRITE OPERATIONS

(A) BYTE WRITE

A byte write operation starts when a micro-controller sends a START bit condition, follows by a proper EEPROM device address and then a write command. If the device address bits match the chip select address, the EEPROM device will acknowledge at the 9th clock cycle. The micro-controller will then send the rest of the lower 8 bits word address. At the 18th cycle, the EEPROM will acknowledge the 8-bit address word. The micro-controller will then transmit the 8 bit data. Following an ACKNOWLDEGE signal from the EEPROM at the 27th clock cycle, the micro-controller will issue a STOP bit. After receiving the STOP bit, the EEPROM will go into a self-timed programming mode during which all external inputs will be disabled. After a programming time of T_{WC}, the byte programming will finish and the EEPROM device will return to the STANDBY mode.

(B) PAGE WRITE

A page write is similar to a byte write with the exception that one to sixteen bytes can be programmed along the same page or memory row. All FT24C02/04/08/16 are organized to have 16 bytes per memory row or page.

With the same write command as the byte write, the micro-controller does not issue a STOP bit after sending the 1st byte data and receiving the ACKNOWLEDGE signal from the EEPROM on the 27th clock cycle. Instead it sends out a second 8-bit data word, with the EEPROM acknowledging at the 36th cycle. This data sending and EEPROM acknowledging cycle repeats until the micro-controller sends a STOP bit after the $n \times 9^{th}$ clock cycle. After which the EEPROM device will go into a self-timed partial or full page programming mode. After the page programming completes after a time of T_{WC}, the devices will return to the STANDBY mode.

The least significant 4 bits of the word address (column address) increments internally by one after receiving each data word. The rest of the word address bits (row address) do not change internally, but pointing to a specific memory row or page to be programmed. The first page write data word can be of any column address. Up to 16 data words can be loaded into a page. If more then 16 data words are loaded, the 17th data word will be loaded to the 1st data word column address. The 18th data word will

be loaded to the 2nd data word column address and so on. In other word, data word address (column address) will "roll" over the previously loaded data.

(C) ACKNOWLEDGE POLLING

ACKNOWLEDGE polling may be used to poll the programming status during a self-timed internal programming. By issuing a valid read or write address command, the EEPROM will not acknowledge at the 9th clock cycle if the device is still in the self-timed programming mode. However, if the programming completes and the chip has returned to the STANDBY mode, the device will return a valid ACKNOWLEDGE signal at the 9th clock cycle.

READ OPERATIONS

The read command is similar to the write command except the 8th read/write bit in address word is set to "1". The three read operation modes are described as follows:

(A) CURRENT ADDRESS READ

The EEPROM internal address word counter maintains the last read or write address plus one if the power supply to the device has not been cut off. To initiate a current address read operation, the micro-controller issues a START bit and a valid device address word with the read/write bit (8th) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. The internal address word counter will then automatically increase by one. For current address read the micro-controller will not issue an ACKNOWLEDGE signal on the 18th clock cycle. The micro-controller issues a valid STOP bit after the 18th clock cycle to terminate the read operation. The device then returns to STANDBY mode.

(B) SEQUENTIAL READ

The sequential read is very similar to current address read. The micro-controller issues a START bit and a valid device address word with read/write bit (8th) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. Meanwhile the internally address word counter will then automatically increase by one. Unlike current address read, the micro-controller sends an ACKNOWLEDGE signal on the 18th clock cycle signaling the EEPROM device that it wants another byte of data. Upon receiving the ACKNOWLEDGE signal, the EEPROM will serially clocked out an 8-bit data word based on the incremented internal address counter. If the micro-controller needs another data, it sends out an ACKNOWLEDGE signal on the 27th clock cycle. Another 8-bit data word will then be serially clocked out. This sequential read continues as long as the micro-controller sends an ACKNOWLEDGE signal after receiving a new data word. When the internal address counter reaches its maximum valid address, it rolls over to the beginning of the memory array address. Similar to current address read, the micro-controller can terminate the sequential read by not acknowledging the last data word received, but sending a STOP bit afterwards instead.

(C) RANDOM READ

Random read is a two-steps process. The first step is to initialize the internal address counter with a target read address using a "dummy write" instruction. The second step is a current address read.

To initialize the internal address counter with a target read address, the micro-controller issues a START bit first, follows by a valid device address with the read/write bit (8th) set to "0". The EEPROM will then acknowledge. The micro-controller will then send the address word. Again the EEPROM will acknowledge. Instead of sending a valid written data to the EEPROM, the micro-controller performs a current address read instruction to read the data. Note that once a START bit is issued, the EEPROM will reset the internal programming process and continue to execute the new instruction - which is to read the current address.

Figure 3: BYTE WRITE INSTURCTION (SDA INPUT)

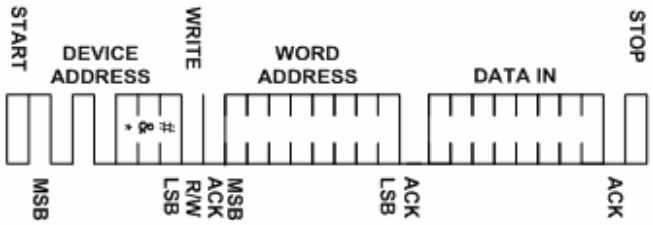
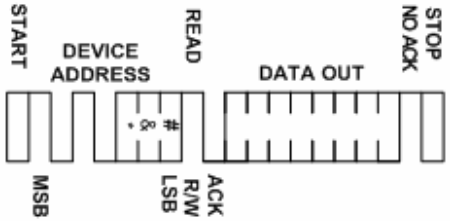


Figure 4: PAGE WRITE INSTURCTION (SDA INPUT)

Figure 5: CURRENT ADDRESS READ (SDA INPUT/OUTPUT)



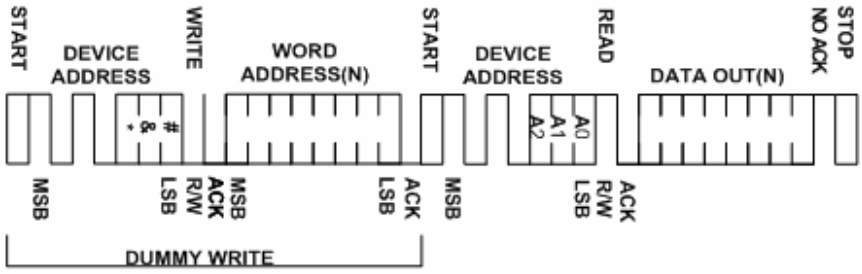
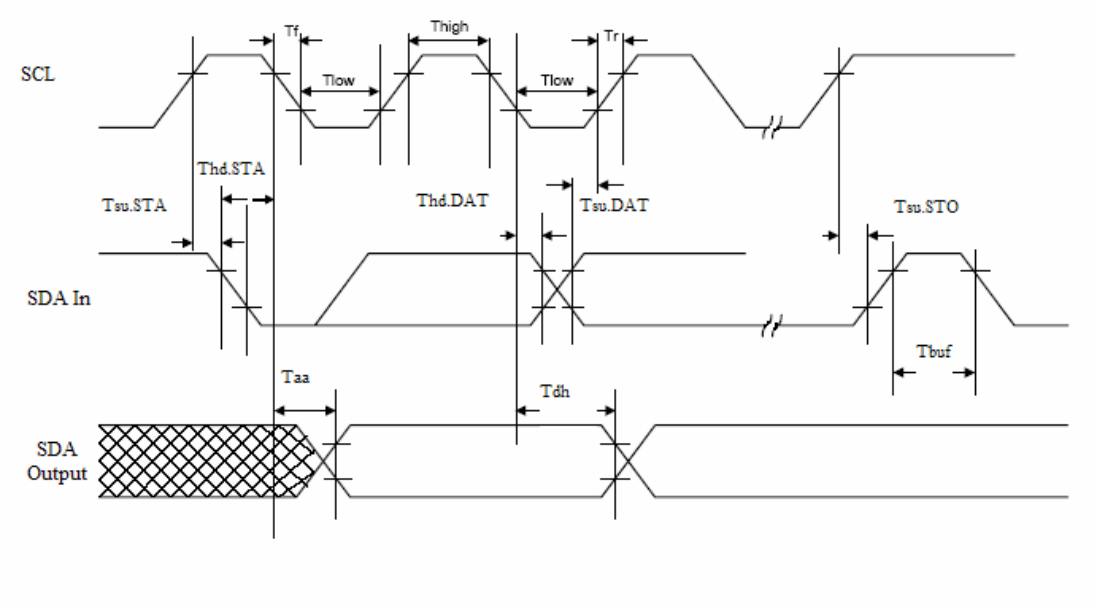


Figure 7: SEQUENTIAL READ (SDA INPUT/OUTPUT)

Notes: 1) * = Pin A2 for FT24C02/04/08 and FT24C02A/04A/08A
& = Pin A1 for FT24C02/04 and FT24C02A/04A
# = Pin A0 for FT24C02 and FT24C02A

Figure 8: SCL and SDA Bus Timing



AC CHARACTERISTICS

	Parameter	FT24C 02A / 04A / 08A / 16A		FT24C 02 / 04 / 08 / 16		FT24C 02A / 04A / 08A / 16A 02 / 04 / 08 / 16		Unit
		1.8 V		2.5 V		5.5 V		
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock frequency, SCL		100		400		400	kHz
t_{LOW}	Clock pulse width low	4.7		1.2		1.2		µs
t_{HIGH}	Clock pulse width high	4.0		0.6		0.6		µs
t_I	Noise suppression time		100		50		50	ns
t_{AA}	Clock low to data out valid	0.1	4.5	0.1	0.9	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		1.2		1.2		µs
$t_{HD.STA}$	START hold time	4.0		0.6		0.6		µs
$t_{SU.STA}$	START set-up time	4.7		0.6		0.6		µs
$t_{HD.DAT}$	Data in hold time	0		0		0		µs
$t_{SU.DAT}$	Data in set-up time	200		100		100		µs
t_R	Input rise time		1		0.3		0.3	µs
t_F	Input fall time		300		300		300	ns
$t_{SU.STO}$	STOP set-up time	4.7		0.6		0.6		µs
t_{DH}	Date out hold time	100		50		50		ns
t_{WR}	Write cycle time		5		5		5	ms

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
V_{CC1}	24C××A supply V_{CC}		1.8		5.5	V
V_{CC1}	24C×× supply V_{CC}		2.5		5.5	V
I_{CC}	Supply read current	V_{CC} @ 5.0V SCL = 100 kHz		0.5	1.0	mA
I_{CC}	Supply write current	V_{CC} @ 5.0V SCL = 100 kHz		2.0	3.0	mA
I_{SB1}	Supply current	V_{CC} @ 1.8V, V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB2}	Supply current	V_{CC} @ 2.5V, V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB3}	Supply current	V_{CC} @ 5.0V, V_{IN} = V_{CC} or V_{SS}		0.07	1.0	µA
I_{IL}	Input leakage current	V_{IN} = V_{CC} or V_{SS}			3.0	µA
I_{LO}	Output leakage current	V_{IN} = V_{CC} or V_{SS}			3.0	µA
V_{IL}	Input low level		-0.6		V_{CC} × 0.3	V
V_{IH}	Input high level		V_{CC} × 0.7		V_{CC} + 0.5	V
V_{OL2}	Output low level	V_{CC} @ 3.0V, I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output low level	V_{CC} @ 1.8V, I_{OL} = 0.15 mA			0.4	V