1.54 inch
E-paper Display Series

GooDisplay®

GDEW0154M09

Dalian Good Display Co., Ltd.

Product Specifications

Customer	**Standard**
Description	**1.54” E-PAPER DISPLAY**
Model Name	**GDEW0154M09**
Date	**2020/07/09**
Revision	**2.1**

	Design Engineering		
	Approval	**Check**	**Design**
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Revision History

Rev.	Issued Date	Revised Contents
1.0	Dec.12.2019	Preliminary
2.0	Feb.18.2020	Update 1.4 Mechanical Drawing of EPD module
2.1	July.09.2020	Update 1.4 Mechanical Drawing of EPD module

GOOD DISPLAY

1. General Description

1.1 Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 1.54" active area contains 200×200 pixels, and has 1-bit white/black full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

1.2 Features

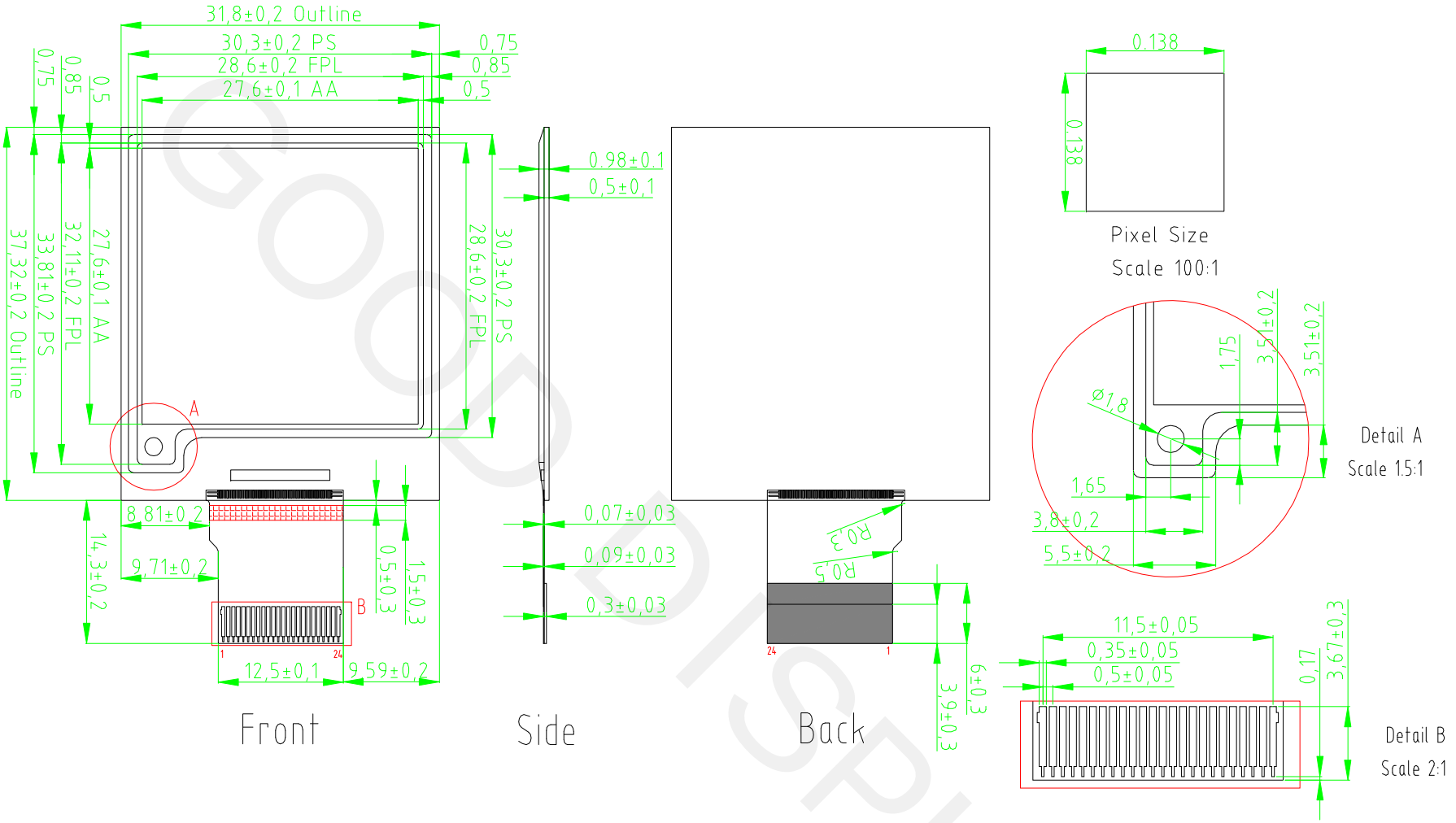
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 230um

1.3 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.54	Inch	
Display Resolution	200(H)×200(V)	Pixel	Dpi:184
Active Area	27.6(H)×27.6(V)	mm	
Pixel Pitch	0.138×0.138	mm	
Pixel Configuration	Square		
Outline Dimension	31.80(H)×37.32(V) ×0.98(D)	mm	
Weight	2.5±0.5	g	

GOOD DISPLAY

This drawing is a confidential document.
It is forbidden to copy or disclose the information without the written authorization of Dalian Good Display Co., LTD.



Note:

1. Resolution:200(G)*200(S)
2. DPI:184
3. Unlabeled tolerances:±0.15

					DALIAN GOOD DISPLAY CO.,LTD.
					File Serial Number: GDEW0154M09
MARK:	CHANGE CONTENT		SIGNATURE	DATE	WF P/N: GDEW0154M09
DRAWN:		TECHNOLOGY:			SCALE: 1:1 / SIZE: mm / Material:
PROOF-READ		CHECKED:			Version Number: / Publish Date:
STANDARDIZATION		APPROVALS:			SHEET 1 OF 1

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1.5 Input/Output Terminals

1.5-1) Pin out List

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I^2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I^2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 1.5-5
9	O	BUSY	Busy state output pin	Note 1.5-4
10	I	RES #	Reset	Note 1.5-3
11	I	D/C #	Data /Command control pin	Note 1.5-2
12	I	CS #	Chip Select input pin	Note 1.5-1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19	C	VPP	Power Supply for OTP Programming	
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

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Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

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1.6 Reference Circuit

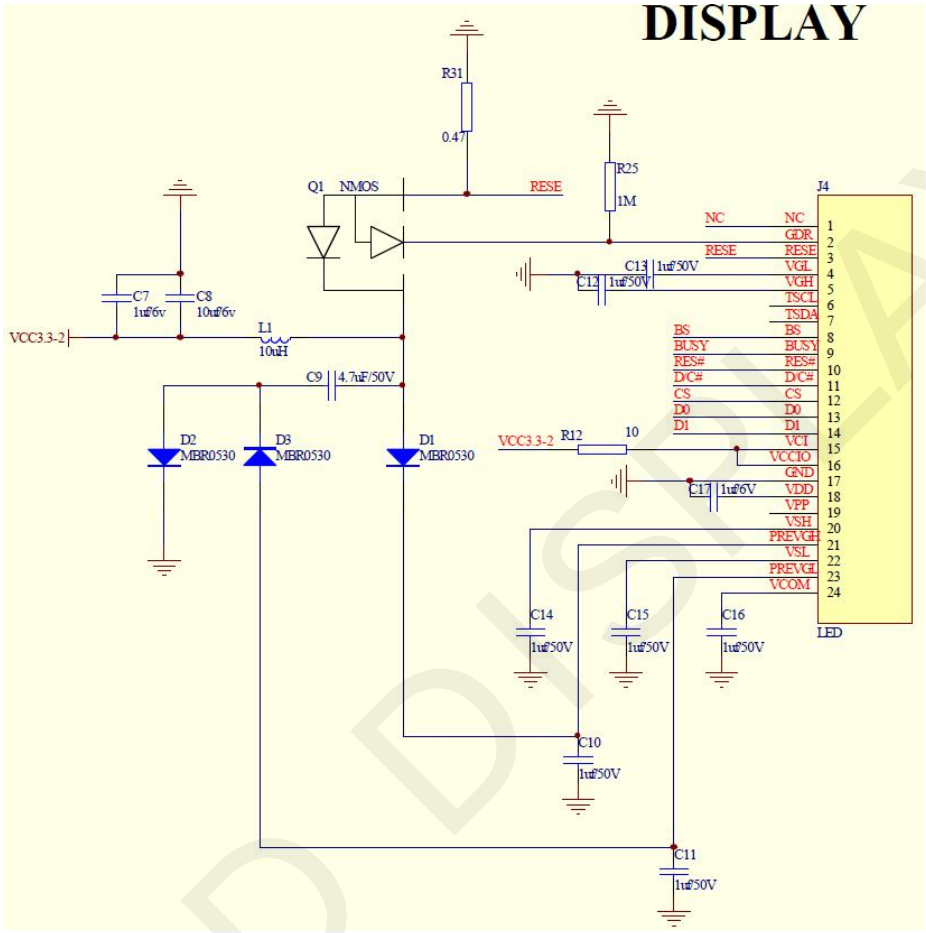

Figure . 1.6-5 (1)

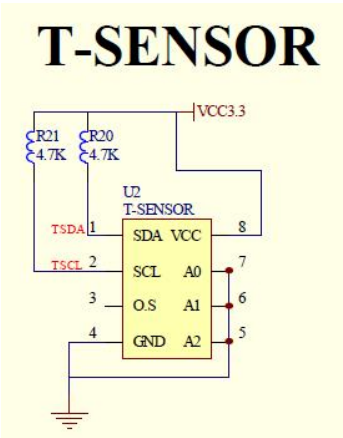

Figure . 1.6-5 (2)

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1.7 Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display and three-color (black, white and red/Yellow) Good Display ‘s E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.

More details about the Development Kit, please click to the following link:

http://www.good-display.com/companyfile/Development-Board-8

GOOD DISPLAY

2. Environmental

2.1 Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

GOOD DISPLAY

2.2 Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T =50℃,RH=35 % for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
2	Low-Temperature Operation	T = 0℃for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab.	When experiment finished, the EPD must meet electrical and optical performance standards.
3	High-Temperature Storage	T=+70℃, RH=35% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab	When experiment finished, the EPD must meet electrical and optical performance standards.
5	High Temperature, High-Humidity Operation	T=+40℃, RH=80% For 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical and optical performance standards.
6	High Temperature, High-Humidity Storage	T=+60℃, RH=80% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical performance standards.

7	Temperature Cycle	[-25℃ 30mins]→ [+70℃, RH=35% 30mins],70cycles Test in white pattern	1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25℃, storage period 30 minutes. After 30 minutes, it needs 30min to let temperature rise to 70℃. After 30min, temperature will be adjusted to 70℃, RH=35%, and storage period is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25℃. One temperature cycle (2hrs) is complete. 2. Temperature cycle repeats 70 times. 3. When 70 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As EPDs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-14NB.	When experiment finished, the EPD must meet electrical and optical performance standards.
8	UV exposure Resistance	765 W/m^2 for 168 hrs,40℃	Standard # IEC 60 068-2-5 Sa	
9	Electrostatic discharge	Machine model: +/-250V, 0Ω,200pF	Standard # IEC61000-4-2	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note:

(1) The protective film must be removed before temperature test.

(2) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 4 hours at 25℃.

3. Electrical Characteristics

3.1 Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.3 to +6.0	V
Logic Input Voltage	V_{IN}	-0.3 to VCI +2.4	V
Operating Temp. range	T_{OPR}	0 to +50	℃
Storage Temp. range	T_{STG}	-25 to +70	℃
Humidity range	-	40~70	%RH

***Note: Avoid direct sunlight.**

3.2 Panel DC Characteristics

The following specifications apply for: VSS = 0V, VCI = 3.3V, TA = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	VCI	-	2.3	3.3	3.6	V
High level input voltage	VIH	Digital input pins	0.7VCI	-	VCI	V
Low level input voltage	VIL	Digital input pins	0	-	0.3VCI	V
High level output voltage	VOH	Digital input pins , IOH= 400uA	VCI-0.4	-	-	V
Low level output voltage	VOL	Digital input pins , IOL= -400uA	0	-	0.4	V
Image update current	I_{UPDATE}	-	-	1	3	mA
Standby panel current	Istandby	-	-	-	5	uA
Power panel (update)	P_{UPDATE}	-	-	6.6	18	mW
Standby power panel	P_{STBY}	-	-	-	0.0165	mW
Operating temperature	-	-	0	-	50	℃
Storage temperature	-	-	-25	-	70	℃
Image update Time at 25 ℃	-	-	-	2	4	Sec
Deep sleep mode current	I_{VCI}	DC/DC off No clock No input load Ram data not retain	-	2	5	uA
Sleep mode current	I_{VCI}	DC/DC off No clock No input load Ram data retain	-	35	50	uA

- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display
- Vcom is recommended to be set in the range of assigned value ± 0.1V.

3.3 Panel AC Characteristics

3.3-1) Oscillator frequency

The following specifications apply for : VSS = 0V, VCI = 3.3V, TA = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator frequency	Fosc	VCI=2.3 to 3.6V	-	1.625	-	MHz

3.3-2) MCU Interface

3.3-2-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDIN	SCLK	CS#	D/C#	RES#
SPI3	SDIN	SCLK	CS#	L	RES#

Table 3-1: MCU interface assignment under different bus interface mode

Note 3-1: L is connected to VSS

Note 3-2: H is connected to VCI

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3.3-2-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 3-2: Control pins of 4-wire Serial Peripheral interface

Note 3-3: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

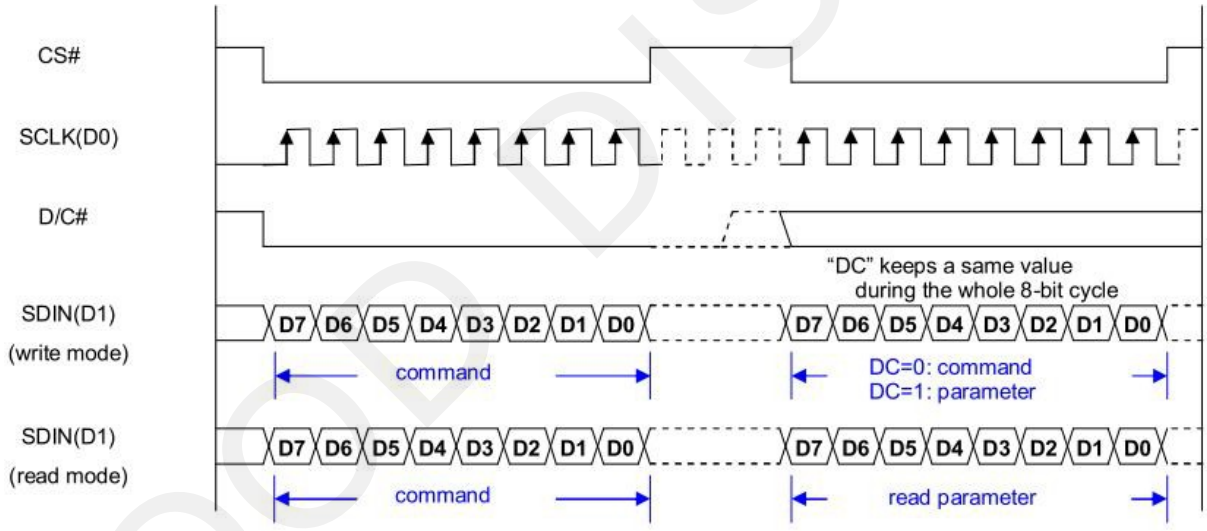

Figure 3-1: Write procedure in 4-wire Serial Peripheral Interface mode

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3.3-2-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data ADIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Table 3-3: Control pins of 3-wire Serial Peripheral Interface

Note 3-4: ↑stands for rising edge of signal

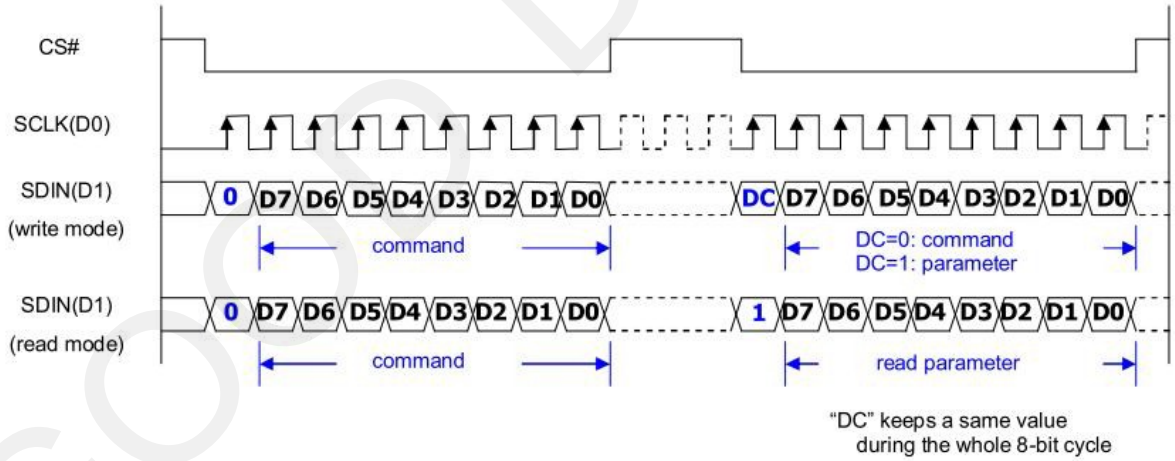
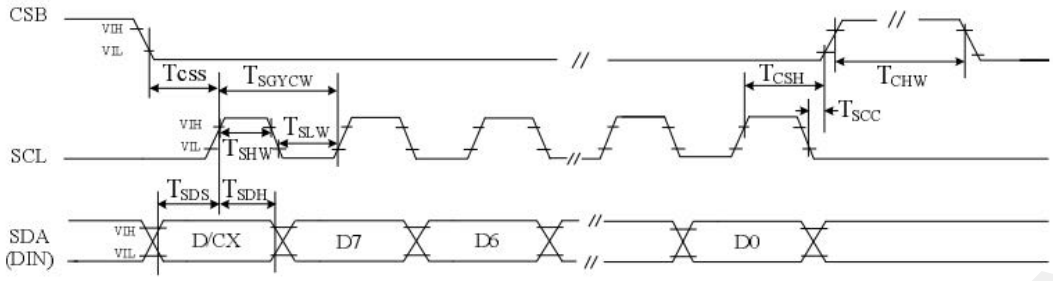
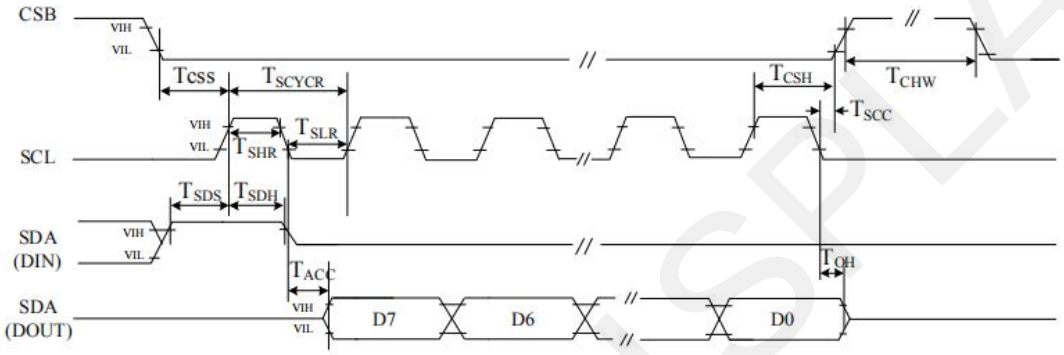


Figure 3-2: Write procedure in 3-wire Serial Peripheral Interface mode

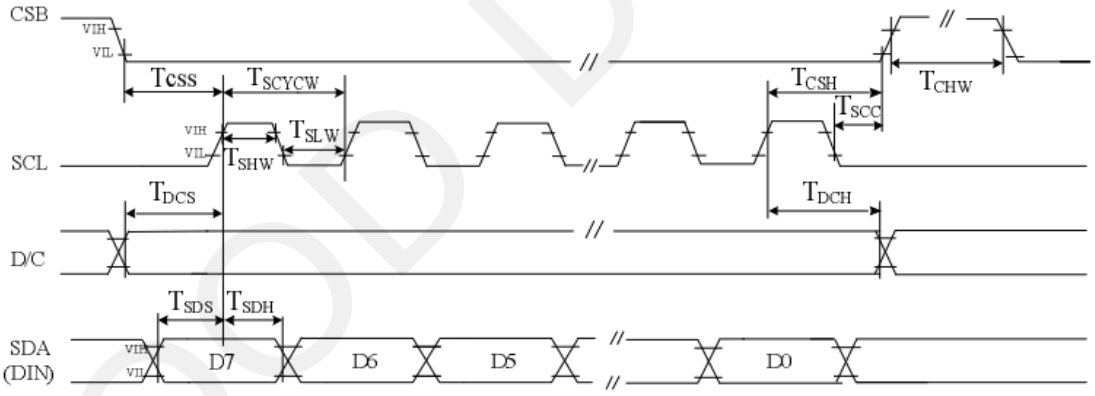
3.3-3) Timing Characteristics of Series Interface



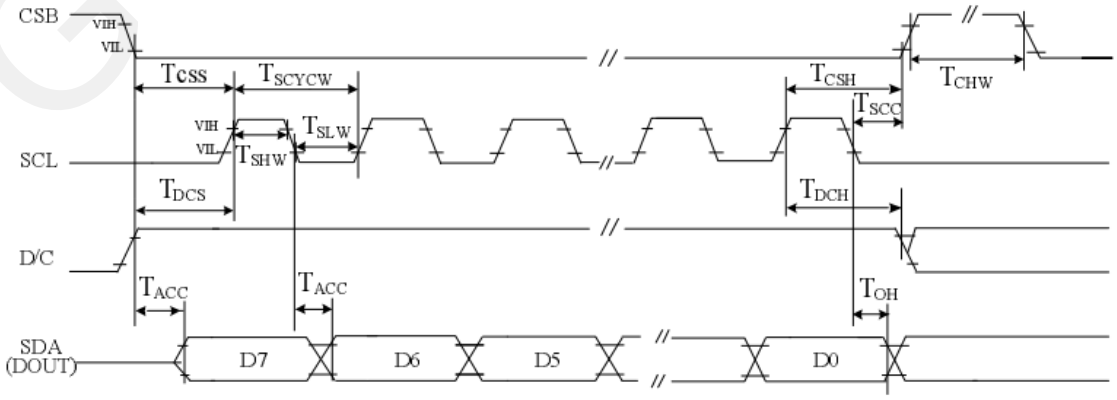
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)

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Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CS#	Chip Select Setup Time	60	-	-	ns
tcsh		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	40	-	-	ns
tscycw	SCL	Serial clock cycle (write)	100	-	-	ns
tshw		SCL “H” pulse width (write)	35	-	-	ns
tslw		SCL“L” pulse width (write)	35	-	-	ns
tscycr		Serial clock cycle (Read)	150	-	-	ns
tshr		SCL “H” pulse width (Read)	60	-	-	ns
tslr		SCL “L” pulse width (Read)	60	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc		Access time	-	-	50	ns
toh		Output disable time	15	-	-	ns

3.4 Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	6.6	18	mW	-
Power consumption in standby mode	-	25℃	-	0.0165	mW	-

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4. Typical Operating Sequence

TBD

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5. Command Table

W/R: 0: Write cycle 1: Read cycle D/CX: 0: Command 1: Data D7~D:-: Don't care

Address	Command	Bit										
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0		0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	0Fh
		W	1	-	-	-	VCMZ	TS_AUTO	VGLTIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	0Ah
		W	1			-	VCOM_HV -	VGHL_LV [1]	VGHL_LV [0]	VGHL_LV [1]	VGHL_LV [0]	39h
		W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	39h
		W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26h
		W	1	OPTEN	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	06h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	-	-	T_VDS_OFF[1]	T_VDS_OFF[0]	T_VSHR_OFF [1]	T_VSHR_OFF[0]	-	-	00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R05H	Power ON Measure (PMES)	W	0	0	0	0	0	0	1	0	1	05H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	BT_PHA[7]	BT_PHA[6]	BT_PHA[5]	BT_PHA[4]	BT_PHA[3]	BT_PHA[2]	BT_PHA[1]	BT_PHA[0]	17h
		W	1	BT_PHB[7]	BT_PHB[6]	BT_PHB[5]	BT_PHB[4]	BT_PHB[3]	BT_PHB[2]	BT_PHB[1]	BT_PHB[0]	17h
		W	1	-	-	BT_PHC[5]	BT_PHC[4]	BT_PHC[3]	BT_PHC[2]	BT_PHC[1]	BT_PHC[0]	17h
		W	1	1	0	1	0	0	1	0	1	A5h
		W	1	FT_PHC[3]	FT_PHC[2]	FT_PHC[1]	FT_PHC[0]	FT_PHB[3]	FT_PHB[2]	FT_PHB[1]	FT_PHB[0]	00h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission1 (DTM1)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
R13H	Data Start transmission 2(DTM2)	W	0	0	0	0	1	0	0	1	1	13H
		W	1	#	#	#	#	#	#	#	#	00h
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R18H	BIST	W	1	0	0	0	1	1	0	0	0	18H
		W	1	0	0	0	0	0	0	0	0	00h
		W	1	0	0	0	0	0	0	0	0	00h
R19H	BIST_PS	W	1	0	0	0	1	1	0	0	1	19H

		W	1	0	0	0	0	0	0	0	0	00h
		W	1	W [7:3]								00h
		W	1	L[7:0]								00h
		W	1	X1[7:3]					0	0	0	00h
		W	1	Y1[7:0]								00h
		W	1	X2[7:3]					1	1	1	00h
		W	1	Y2[7:0]								00h
R20H	LUT for VCOM (LUT1)	W	0	0	0	1	0	0	0	0	0	20H
		W	1	#	#	#	#	#	#	#	#	00h
R21H	White to White LUT (LUTWW)	W	0	0	0	1	0	0	0	0	1	21H
		W	1	#	#	#	#	#	#	#	#	00h
R22H	Black to White LUT (LUTBW/LUTR)	W	0	0	0	1	0	0	0	1	0	22H
		W	1	#	#	#	#	#	#	#	#	00h
R23H	White to Black LUT (LUTWB/LUTW)	W	0	0	0	1	0	0	0	1	1	23H
		W	1	#	#	#	#	#	#	#	#	00h
R24H	Black to Black LUT (LUTBB/LUTB)	W	0	0	0	1	0	0	1	0	0	24H
		W	1	#	#	#	#	#	#	#	#	00h
R25H	Group frame rate	W	0	0	0	1	0	0	1	0	1	25H
		W	1			Group1 M[2:0]			Group1 N[2:0]			3ch
		W	1			Group2 M[2:0]			Group2 N[2:0]			3ch
		W	1			Group3 M[2:0]			Group3 N[2:0]			3ch
		W	1			Group4 M[2:0]			Group4 N[2:0]			3ch
		W	1			Group5 M[2:0]			Group5 N[2:0]			3ch
		W	1			Group6 M[2:0]			Group6 N[2:0]			3ch
		W	1			Group7 M[2:0]			Group7 N[2:0]			3ch
		W	1			Group8 M[2:0]			Group8 N[2:0]			3ch
R26H	Set LUT States (SET_GROUP)	W	0	0	0	1	0	0	1	1	0	26H
		W	1	0	0	0	0	0	0	0	0	00h
R2AH	LUTC option	W	0	0	0	1	0	0	1	0	1	2AH
		W	1	EOPT	-	-	-	-	-	-	-	00h
		W	1	STATE_XON[7:0]								00h
		W	1	STATE_XON[15:8]								00h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-		M[2:0]			N[2:0]			3Ah
R31H	PLL mode selection	W	0	0	0	1	1	0	0	0	1	31H
		W	1	0	0	0	0	0	0	0	PLL option	01h
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]	--
		R	1	D2/TS[1]	D1/TS[0]	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO0]	00h

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R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	--
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	--
R44H	Panel Glass Check (PBC)	W	0	0	1	0	0	0	1	0	0	44H
		R	1	-	-	-	-	-	-	-	PSTA	-
R50H	VCOM and DATA interval setting	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	GHD	SHD	SLD	SHRD-	-	-	-	LPD	--
R60H	TCON setting (TCON)	W	0	0	1	1	0	0	0	0	0	60H
		W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	-	-	-	00h
		W	1	-	-	-	-	-	-	-	VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R65H	Gate/Source Start Setting (GSST)	W	0	0	1	1	0	0	0	1	0	65H
		W	1	S_start (7)	S_start (6)	S_start (5)	S_start (4)	S_start (3)	-	-	-	00h
		W	1				gscan				G_start [8]	00h
		W	1	G_start (7)	G_start (6)	G_start (6)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	00h
R68H	Internal VOTP	W	0	0	1	1	0	1	0	0	0	68H
		W	1	Internal VOTP[7:0]								00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	--
		R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV10]	REV[09]	REV[08]	--
		R	1	Vendor ID				CHIP_REV				--
R71H	Status register(FLG)	W	0	0	1	1	1	0	0	0	1	71H
		R	1	Con_fb	PTL_flag	I2C_ERR	I2C_ BUSYN	Data_flag	PON	POF	BUSY_N	-
R7FH	Read Reserved Bytes	W	0	0	1	1	1	1	1	1	1	7FH
		R	1	#	#	#	#	#	#	#	#	
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	-	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h
R90H	Partial Window (PTL)	W	0	1	0	0	1	0	0	0	0	90H
		W	1	HRST[7:3]				0	0	0	00h	00h

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		W	1	HRED[7:3]				1	1	1	00h	00h
		W	1	-	-	-	-	-	-	-	VRST[8]	00h
		W	1	VRST[7:0]								00h
		W	1	-	-	-	-	-	-	-	VRED[8]	00h
		W	1	VRED[7:0]								00h
		W	1	-	-	-	-	-	-	-	PT_SCA	00h
R91H	Partial In(PTIN)	W	0	1	0	0	1	0	0	0	1	91H
R92H	Partial Out(PTOUT)	W	0	1	0	0	1	0	0	1	0	92H
R94H	CRCS	W	0	1	0	0	1	0	1	0	0	94H
R95H	CRCO	W	0	1	0	0	1	0	1	0	1	95H
R96H	CRC status read	W	0	1	0	0	1	0	1	1	0	96H
		R	1	CRC_MSB[7:0]								-
		R	1	CRC_LSB[7:0]								-
R97H	Write OTP key	W	0	1	0	0	1	0	1	1	1	97H
		W	1	CRC_MSB[7:0]								-
		W	1	CRC_LSB[7:0]								-
RA0H	Program Mode(PGM)	W	0	1	0	1	0	0	0	0	0	A0H
RA1H	Active Program (APG)	W	0	1	0	1	0	0	0	0	1	A1H
RA2H	Read OTP Data (ROTP)	W	0	1	0	1	0	0	0	1	0	A2H
		R	1	#	#	#	#	#	#	#	#	--
RE0H	CASCADE setting (CCSET)	W	0	1	1	1	0	0	0	0	0	E0H
		W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h
RE1H	Set OTP program bank (SET_OTP_BANK)	W	0	1	1	1	0	0	0	0	1	E1H
		W	1	-	-	-	-	-	-	LUT_bank0	reg_bank0	03h
RE3H	Power saving	W	0	1	1	1	0	0	0	1	1	E3H
		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h
RE4H	LVD voltage Select	W	0	1	1	1	0	0	1	0	0	E4H
		W	1	-	-	-	-	-	-	LVD_SEL [1]	LVD_SEL [0]	03h
RE5H	Force Temperature	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

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(1) Panel Setting (PSR) (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	REG_EN	BWR	UD	SHL	SHD_N	RST_N
	0	1	-	-	-	VCMZ	TS_AUTO	VGLTIEG	NORG	VC_LUTZ

RES[1:0]: Display Resolution setting (source x gate)

11: Display resolution is 200x200 Others: no define.

REG_EN: LUT selection

0: LUT from OTP. (Default)

1: LUT from register.

BWR: Color selection setting

0: Pixel with Black/White/Red, BWR mode. (Default)

1: Pixel with Black/White, BW mode.

UD: UD function

0: Scan down. First line to last line: Gn → Gn-1 → Gn-2 → ... → G1

1: Scan up. (default) First line to last line: G1 → G2 → G3 → ... → Gn

SHL: SHL function

0: Shift left First data to last data: Sn → Sn-1 → Sn-2 → ... → S1

1: Shift right. (default) First data to last data: S1 → S2 → S3 → ... → Sn

SHD_N: SHD_N function

0: Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating.

1: Booster ON (Default)

When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.

RST_N: RST_N function

0: Booster OFF, Register data are set to their default values, and SEG/BG/ VCOM floating.

1: No effect (Default).

When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.

VCMZ : VCOM status function

0 : No effect (default) 1 : VCOM is always floating

GOOD DISPLAY

TS_AUTO : Temperature sensing will be activated automatically one time

0 : Before enabling refresh, temperature sensing on

1 : Before enabling booster, temperature sensing on (default)

VGLTIEG : VGL power off status function

0 : Power off, VGL will be floating (default)

1 : Power off, VGL will be tied to GND

NORG : VCOM status function

0 : No effect (default)

1 : Expect refreshing display, VCOM is tied to GND

VC_LUTZ : VCOM status function

0 : Display off, VCOM keep to power off

1 : Display off, VCOM is set to floating (default)

(2) Power Setting (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External	0	0	0	0	0	0	0	0	0	1
Power	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN
	0	1	-	-	-	VCOM_HV	VGHL_LV[3:0]			
	0	1	-	-	VSH[5:0]					
	0	1	-	-	VSL[5:0]					
	0	1	OPTEN	VSHR[6:0]						

VDS_EN: Source power selection

0: External source power from VSH/VSL/VSHR pins.

1: Internal DC/DC function for generating VSH/VSL/VSHR. (Default)

VDG_EN: Gate power selection

0: External VDNS power from VGH/VGL pins. (VDNG_EN open)

1: Internal DC/DC function for generating VGH/VGL. (default)

VCOM_HV: VCOM Voltage Level

0: VCOMH=VSH+VCOMDC (default), VCOML=VSL+VCOMDC

1: VCOML=VGH, VCOML=VGL

VGHL_LV[3:0]: VGH / VGL Voltage Level selection.

GOODDISPLAY

VGHL_LV	VGHL voltage level	VGHL_LV	VGHL voltage level
0000	VGH=10V,VGL= -10V	....	....
0001	VGH=11V,VGL= -11V	0001	VGH=20V,VGL= -20V
0010	VGH=12V,VGL= -12V	0010	VGH=21V,VGL= -21V
0011	VGH=13V,VGL= -13V	1100	VGH=22V,VGL= -22V

VSH[5:0]: Internal VSH power selection for B/W pixel.(Default value: 100110b)

VSH[5:0]	VSH_V	VDH	VSH_V
000000	3.6V	...	...
000001	3.8V	110100	14.0V
000010	4V	110101	14.2V
000011	4.2V	110110	14.4V
000100	4.4V	110111	14.6V
000101	4.6V	111000	14.8V
000110	4.8V	111001	15.0V
000111	5.0V	(others)	15.0V

VSL[5:0]: Internal VSL power selection for B/W pixel.

VSL	VSL_V	VSL	VSL_V
000000	-3.6V	...	...
000001	-3.8V	110100	-14.0V
000010	-4.0V	110101	-14.2V
000011	-4.2V	110110	-14.4V
000100	-4.4V	110111	-14.6V
000101	-4.6V	111000	-14.8V
000110	-4.8V	111001	-15.0V
000111	-5.0V	(others)	-15.0V

VSHR[5:0]: Internal VSHR power selection.

VSHR	VSHR _V	VSHR	VSHR _V
000000	2.4V	...	...
000001	2.6V	111001	13.8V
000010	2.8V	111010	14.0V
000011	3.0V	111011	14.2V
000100	3.2V	111100	14.4V
000101	3.4V	111101	14.6V
000110	3.6V	111111	15.0V
000111	3.8V	(others)	

OPTEN=1:enable step -0.1 voltage selection(2.4~15V)

Internal VSHR power selection for Red LUT.

GOODDISPLAY

VSHR	VSHR _V	VSHR	VSHR _V
0000000	2.4V	…	…
0000001	2.5V	1111001	14.5V
0000010	2.6V	1111010	14.6V
0000011	2.7V	1111011	14.7V
0000100	2.8V	1111100	14.8V
0000101	2.9V	1111101	14.9V
0000110	3.0V	1111111	15.0V
0000111	3.1V	(others)	

Note: VSH>VSHR

(3) Power OFF (PWR) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the	0	0	0	0	0	0	0	0	1	0

After power off command, driver will power off base on power off sequence.

After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high.

Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(4) Power off sequence setting (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-

T_VDS_OFF[1:0]: Source to gate Power OFF interval time.

00b: 1frame (Default) 01b: 2 frames 10b: 3frames 11b:4 frame

(5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the Power	0	0	0	0	0	0	0	1	0	0

After power on command, driver will power on base on power on sequence.

After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence, BUSY_N signal will rise from low to high.

(6) Power ON Measure (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1	0	1

If user wants to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power detection (R51H) and temperature measurement. (R40H).

(7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4

100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Driving strength of phase A

000b: period 1 001b: period 2 010b: period 3 011b: period 4

100b: period 5 101b: period 6 110b: period 7 **111b: period 8**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4

100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Driving strength of phase B

000b: period 1 001b: period 2 010b: period 3 011b: period 4

100b: period 5 101b: period 6 110b: period 7 **111b: period 8**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4

100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: period 1 001b: period 2 010b: period 3 011b: period 4

100b: period 5 101b: period 6 110b: period 7 **111b: period 8**

(8) Deep Sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excited if check code = 0xA5.

(9) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Pixel (n-7)	Pixel (n-6)	Pixel (n-5)	Pixel (n-4)	Pixel (n-3)	Pixel (n-2)	Pixel (n-1)	Pixel (n)

The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In BW mode, this command writes “OLD” data to SRAM.

In BWR mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) Data Stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	Data_flag	-	-	-	-	-	-	-

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY signal will become “0”.

(11) Display Refresh (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

The command defines as :While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become “0”.

(12) Data start transmission 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	1	1
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Pixel (n-7)	Pixel (n-6)	Pixel (n-5)	Pixel (n-4)	Pixel (n-3)	Pixel (n-2)	Pixel (n-1)	Pixel (n)

The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes “NEW” data to SRAM.

In B/W/Red mode, this command writes “RED” data to SRAM.

(13) Auto Sequence (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Auto Sequence	0	0	0	0	0	1	0	1	1	1
	0	1	Code[7:0]							

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host’s control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(14) BIST mode (BIST) (R18H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
BIST	0	0	0	0	0	1	0	1	1	1
	0	1	1	0	1	0	0	1	0	1
	0	1	1	0	1	0	0	1	0	1

The command define as follows: This command use only BWR mode.

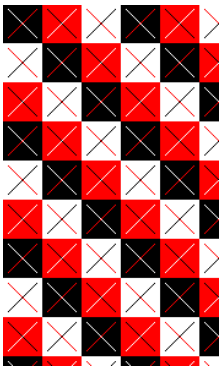
This parameter is a check code.

After this parameter is transmitted, the chip would enter the BIST mode, and display build-in pattern which could be decided by user in R19H (BIST_PS) command.

The command would be excited if check code = 0xA5.

While finished the BIST flow, the check code will be clear to 0x00.

The flow as below: PON→DTM→DSP→POFF



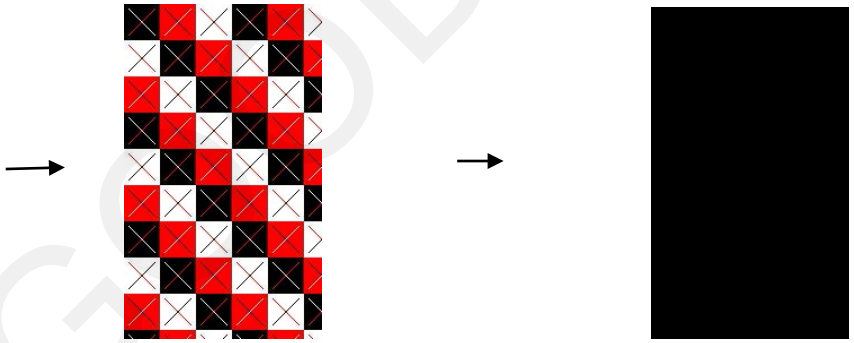
This parameter is a check code.

After this parameter is transmitted, the chip would enter the BIST mode, and display build-in pattern auto run.

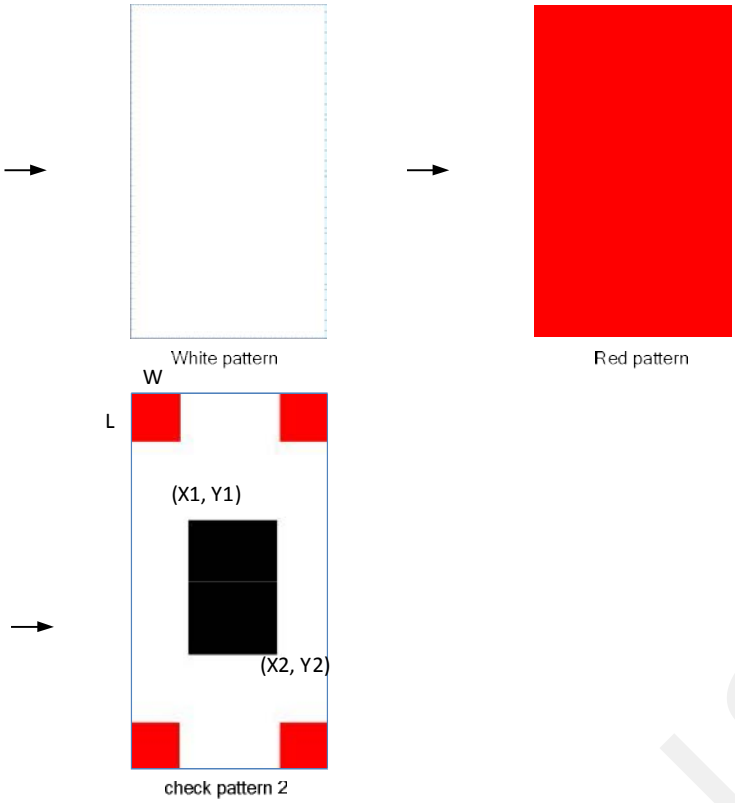
The command would be excited if check code = 0xA5.

The BIST auto run flow will be stop when the check code =0x00.

The flow as below: PON→DTM→DSP→DTM→DSP→...→DTM→DSP→POFF (check code =0x00)



GOOD DISPLAY



This command only actives after hardware reset.

The BUSY flag would change state from 0 to 1 while the command is completed

The DEBUG[6] pin is HW pin control(only auto run)

(15) Pattern Selection in BIST (BIST_PS) (R19H)

Action	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
BIST_PS	W	0	0	0	0	1	1	0	0	1
	W	1	-	-	-	-	-	BSIT_PS[2:0]		
	W	1	W [7:3]					-		
	W	1	L[7:0]							
	W	1	X1[7:3]					0	0	0
	W	1	Y1[7:0]							
	W	1	X2[7:3]					1	1	1
	W	1	Y2[7:0]							

The command can decide which BIST pattern you would like to show.

GOOD DISPLAY

The command can decide which BIST pattern you would like to show.

000: check pattern 001: Black pattern 010: White pattern 011: Red pattern

100: check pattern 2

Note: R19 should be determined before R18.

check pattern 2 setting

W[7:3]: Red block width

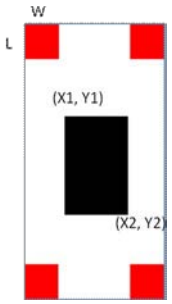
L[7:0]: Red block Length

X1[7:3]: Black block X star point

Y1[7:0]: Black block Y star point

X2[7:3]: Black block X end point

Y2[7:0]: Black block Y end point



Note: 1.W > H/2 W = W/4 2.L > V/2 L = V/4 3.X2 > X1 4.Y2 > Y

(16) LUT for Vcom (LUTC) (R20H)

This command builds Look-up Table for VCOM

(17) W2W LUT (LUTWW) (R21H)

This command builds Look-up Table for White-to-White.

(18) B to W LUT or R LUT (LUTBW/LUTR) (R22H)

This command builds Look-up Table for Black-to-White.

(19) W to B LUT or W LUT (LUTWB/LUTW) (R23H)

This command builds Look-up Table for White - to- Black.

(20) B to B LUT or B LUT (LUTBB / LUTB) (R24H)

This command builds Look-up Table for Black - to- Black.

GOOD DISPLAY

(21) Set LUT each group frame rate (GROUP Frame rate) (R25H)

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
SET_ GROUP	W	0	0	0	1	0	0	1	0	1
	W	1	-	-	Group1 M[2:0]			Group1 N[2:0]		
	W	1			Group2 M[2:0]			Group2 N[2:0]		
	W	1			Group3 M[2:0]			Group3 N[2:0]		
	W	1			Group4 M[2:0]			Group4 N[2:0]		
	W	1			Group5 M[2:0]			Group5 N[2:0]		
	W	1			Group6 M[2:0]			Group6 N[2:0]		
	W	1			Group7 M[2:0]			Group7 N[2:0]		
	W	1			Group8 M[2:0]			Group8 N[2:0]		

The command controls the LUT frequency. The PLL structure must support the following frame rates:

M	N	Frame	M	N	Frame	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

(22) Set LUT States (SET_GROUP) (R26H)

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0
SET_ GROUP	W	0	0	0	1	0	0	1	1	0
	W	1	-	-	-	-	-	-	group_sel[1:0]	

This command is used to set LUT states

Function of group_sel [1:0] are shown below

B/W/Red mode(BWR=0)

Value	Group
00	8
01	7
10	6
11	5

B/W mode (BWR=1)

Value	Group
00	6
01	5
10	4
11	3

(23) LUT Option (LUTOPT) (R2AH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
LUT Option	0	0	0	0	1	0	1	0	1	0
	0	1	EOPT	-	-	-	-	-	-	-
	0	1	STATE_XON[7:0]							
	0	1	STATE_XON[15:8]							

This command sets XON and ending options of source output

STATE_XON[5:0]:

All Gate ON (Each bit controls one state, STATE_XON [0] for state-1, STATE_XON [1] for state-2 …..)

0000 0000 0000 0000b: no All-Gate-ON

0000 0000 0000 0000b: State-1 All-Gate-ON

0000 0000 0000 0000b: State-1 and State2 All-Gate-ON

: :

EOPT: Option for LUT ending

0: Normal.(Default)

1: Source output level keep previous output before power off

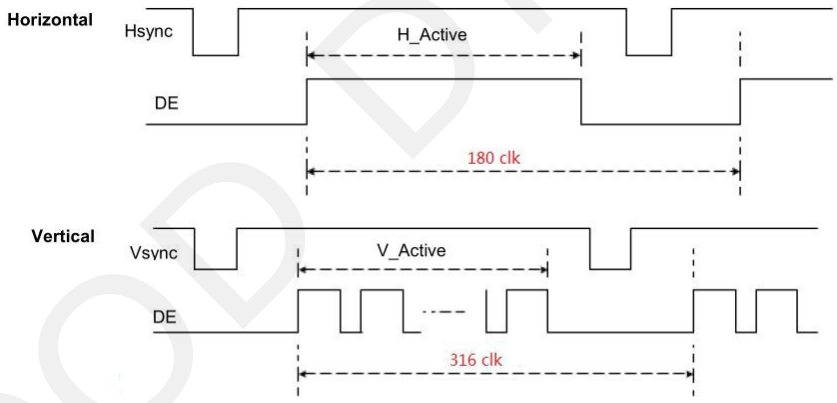
(24) PLL Control (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	M[2:0]			N[2:0]		

GOOD DISPLAY

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame	M	N	Frame	M	N	Frame	M	N	Frame Rate
1	1	29 Hz	3	1	86 Hz	5	1	150 Hz	7	1	200 Hz
	2	14 Hz		2	43 Hz		2	72 Hz		2	100 Hz
	3	10 Hz		3	29 Hz		3	48 Hz		3	67 Hz
	4	7 Hz		4	21 Hz		4	36 Hz		4	50 Hz (Default)
	5	6 Hz		5	17 Hz		5	29 Hz		5	40 Hz
	6	5 Hz		6	14 Hz		6	24 Hz		6	33Hz
	7	4 Hz		7	12Hz		7	20 Hz		7	29 Hz
2	1	57 Hz	4	1	114 Hz	6	1	171 Hz			
	2	29 Hz		2	57 Hz		2	86 Hz			
	3	19 Hz		3	38 Hz		3	57 Hz			
	4	14 Hz		4	29Hz		4	43 Hz			
	5	11 Hz		5	23 Hz		5	34 Hz			
	6	10 Hz		6	19 Hz		6	29 Hz			
	7	8 Hz		7	16 Hz		7	24 Hz			



(25) PLL mode selection (PLL) (R31H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
PLL	0	0	0	0	1	1	0	0	0	1
	0	1	-	-	-	-	-	-	-	PLL option

The command defines as:

The command controls the R30H (PLL)& R25H (group frame rate) selection.

If PLL option sets to 0, R25H (group frame rate) was decided.

If PLL option sets to 1, R30H (PLL) was decided.

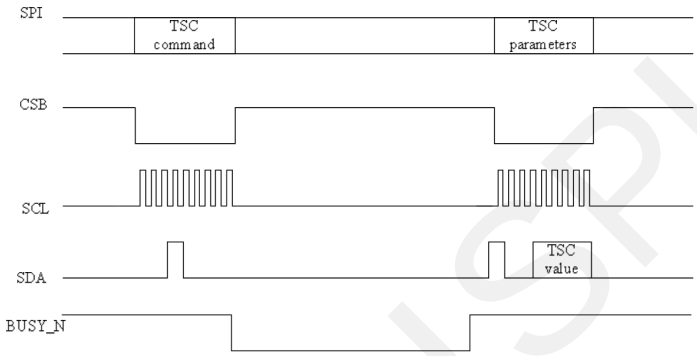
(26) Temperature Sensor Calibration (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS9	D9/TS8	D8/TS7	D7/TS6	D6/TS5	D5/TS4	D4/TS3	D3/TS2
	1	1	D2/TS1	D1/TS0	D0	-	-	-	-	-

This command enables internal the temperaturevalue.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[1:0]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

(27) Temperature Sensor Enable (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enable Temperature Sensor/Offset	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-	TO[5:0]					

This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration

1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-' 2. TO[2:0]: mean temperature offset value

TO[3:0]: Temperature offset.

TO[3:0]	Calculation	TO[3:0]	Calculation
0000 b	0℃(default)	1000	-8℃
0001	1℃	1001	-7℃
0010	2℃	1010	-6℃
…	…	…	…
0110	6℃	1110	-2℃
0111	7℃	1111	-1℃

TO[5:4]: Temperature offset.

TO[5:4]	Calculation	TO[5:4]	Calculation
00 b	0.0℃(default)	10	0.5℃
01	0.25℃	11	075℃

Internal temperature sensor enable

0: Internal temperature sensor enable.(default)

1: Internal temperature sensor disable, using external temperature sensor.

(28) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	1	WLSB[7:0]							

GOOD DISPLAY

This command reads the temperature sensed by the temperature sensor.

WATTR[7:6]: I2C Write Byte Number

00b : 1 byte (head byte only)

01b : 2 bytes (head byte + pointer)

10b : 3 bytes (head byte + pointer + 1st parameter)

11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor.

WLSB[7:0]: LSByte of write-data to external temperature sensor.

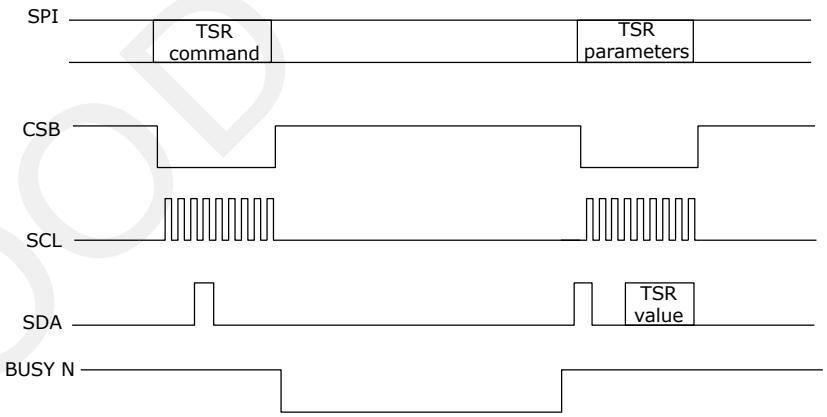
(29) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor



(30) Panel glass check (PBC) (R44H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
PBC	0	0	0	1	0	1	0	0	0	0
	1	1	-	-	-	-	-	-	-	PSTA

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

GOOD DISPLAY

(31) VCOM And Data Interval Setting (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval Between Vcom and Data	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]			

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]:Border data selection

BWR mode (BWR=0)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1(Default)	00	LUTB
	01	LUTR		01	LUTW
	10	LUTW		10	LUTR
	11	LUTB		11(default)	Floating

BW mode (BWR=1)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1(Default)	00	Floating
	01	LUTBW (1→0)		01	LUTWB (0→1)
	10	LUTWB (0→1)		10	LUTBW (1→0)
	11	Floating		11	Floating

Border output voltage level: The level selection is based on mapping LUT data.

Level Selection: 00b: VCOM 01b: VSH 10b: VSL 11b: VSHR

DDX[1:0]: Data polality.

DDX[1] for RED data, DDX[0] for BW data in the BWR mode.

DDX[0] for BW mode.

BWR mode (BWR=0)

DDX[1:0]	Data{Red, B/W}	LUT	DDX[1:0]	Data{Red, B/W}	LUT
00	00	LUTW	10	00	LUTR
	01	LUTB		01	LUTR
	10	LUTR		10	LUTW
	11	LUTR		11	LUTB
01(Default)	00	LUTB	11	00	LUTR
	01	LUTW		01	LUTR
	10	LUTR		10	LUTB
	11	LUTR		11	LUTW

GOOD DISPLAY

B/W mode (BWR=1)

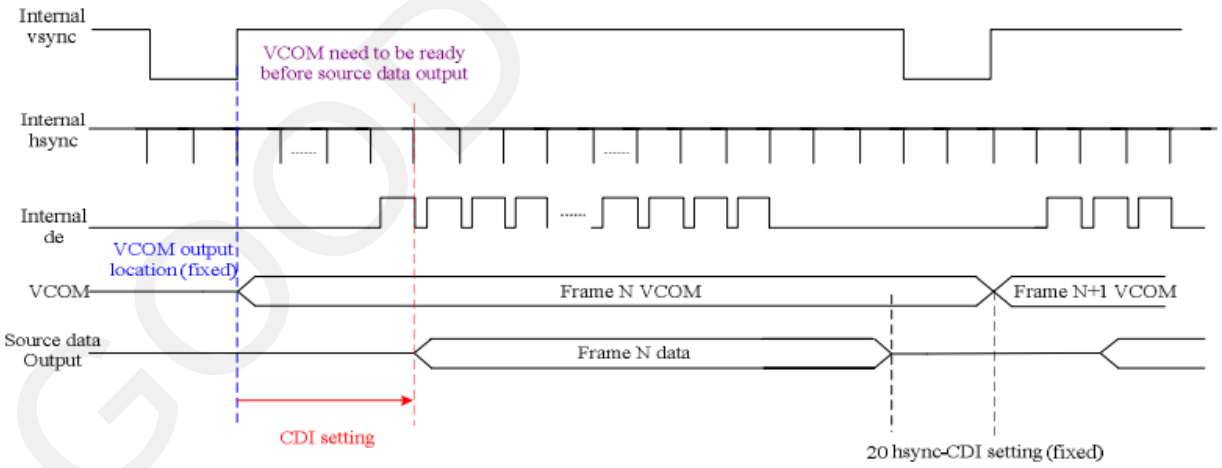
DDX[0]	Data{New, Old}	LUT	DDX[0]	Data{New, Old}	LUT
0	00	LUTWW (0→0)	1(Default)	00	LUTBB (0→0)
	01	LUTBW (1→0)		01	LUTWB (1→0)
	10	LUTWB (0→1)		10	LUTBW (0→1)
	11	LUTBB (1→1)		11	LUTWW (1→1)

DDX[1]=1 is for BW mode without NEW/OLD

DDX[1:0]	Data (B/W)	LUT
10	0	LUTBW(1→0)
	1	LUTWB(0→1)
11	0	LUTWB(0→1)
	1	LUTBW(1→0)

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval	CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync	0110	11
0001	16	0111	10 (Default)
0010	15	...	...
0011	14	1101	4
0100	13	1110	3
0101	12	1111	2



(32) Low Power Detection (LPD) (R51H)

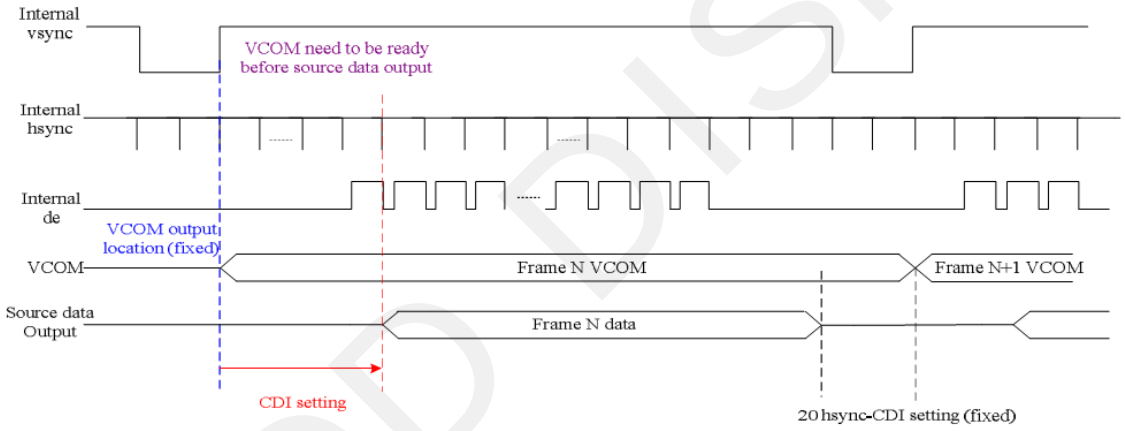
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	GHD	SHD	SLD	SHRD	-	-	-	LPD

This command indicates the input power condition. Host can read this data to understand the battery's condition.

When LPD="1", system input power is normal.

When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)).

Bit	Name	Description
0	LPD	0: Low power input 1: Normal status
4	SHRD	0: Detect voltage < 90%VSHR 1: Normal status
5	SLD	0: Detect voltage < 95%VSL 1: Normal status
6	SHD	0: Detect voltage < 95%VSH 1: Normal status
7	GHD	0: Detect voltage < 95%VGH 1: Normal status



This command only actives after R04H(PON) /R05H(PMES)

(33) TCON Setting (TCON) (R60H)

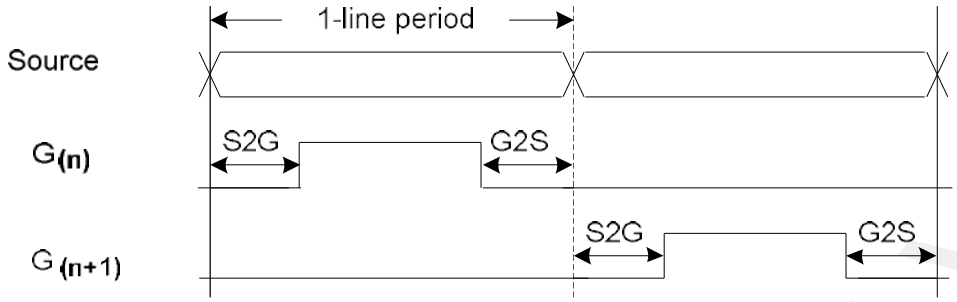
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000b	4		...	...
0001	8		1011	48
0010	12(Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Period = 660 nS.



(34) Resolution Setting (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	HRES[7:3]					0	0	0
	0	1	-	-	-	-	-	-	-	VRES[8]
	0	1	VRES[7:0]							

GOOD DISPLAY

This command defines as follow:

HRES[7:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation:

GD: First active gate = G0 (Fixed); LAST active gate=first active + VRES[8:0] – 1

SD: First active source=S0 (Fixed); LAST active source=first active+HRES[7:3]*8–1

(35) Gate/Source start setting (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1
	0	1	S_start [7:3]					0	0	0
	0	1	-	-	-	gscan	-	-	-	-
	0	1	G_start [7:0]							

The command define as follows:

S_Start [7:3] describe which source output line is the first date line

G_Start[7:0] describe which gate line is the first scan line

gscan :Gate scan select

0: Normal scan 1: Cascade type 2 scan

(36) Internal VOTP (REV) (R68H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
REV	0	0	0	1	1	0	1	0	0	0
	0	1	Internal VOTP[7:0]							

The command can selective external/external VOTP

Cmd.(0x68) + Parameter(0x00) : External VOTP (default)

Cmd.(0x68) + Parameter(0xA7) : Internal VOTP

(37) Revision (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Chip Revision	0	0	0	1	1	1	0	0	0	0
	0	1	REV[7:0]							
	0	1	REV[15:8]							
	0	1	Vendor ID				CHIP_REV			

The LUT_REV is read from OTP address = 0x001/0x801.

The command defines as:

The LUT_REV is read from:

OTP Bank0 address =0xB4C~0xB4D

OTP Bank1 address =0x174C~0x174D

Bit	Description
3-0	CHIP_REV
7-4	Vendor ID: 'F'

(38) Get Status (FLG)(R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	Con_fb	PTL_flag	I^2C_ERR	I^2C_ BUSY	data_ flag	PON	POF	BUSY

This command reads the IC status.

Con_fb: Connector status feedback (high: connection failed), use DEBUG[5] & DEBUG[7]

PTL_FLAG: Partial display status (high: partial mode)

I^2C_ERR: I^2C master error status

I^2C_BUSY: I^2C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY: Driver busy status (low active)

(39) Read Reserved Bytes (RRB) (R7FH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Reserved Bytes	0	0	0	1	1	1	1	1	1	1
	0	1	User reserved byte0							
	0	1	User reserved byte1							
	0	1	User reserved byte2~14							
	0	1	User reserved byte15							

The command defines as: OTP reserved 16 bytes space which user could record more information such as lot number, LUT version….etc.

And the address is 0xB80~0xB8F in bank 0 and 0x1780 ~0x178F in bank1

This command could read these information directly.

GOOD DISPLAY

(40) Auto Measure Vcom (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE

This command reads the IC status.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s 01b: 5s (Default)

10b: 8s 11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)

1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)

1: Source output VSHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value from R81h (default)

1: Get Vcom value in analog signal.

AMVE: Auto Measure Vcom Setting

0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable

(41) Vcom Value (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

This command gets the Vcom value.

VV[5:0]: Vcom Value Output

VV[5:0]	Vcom value
00 0000b	-0.10 V
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

GOOD DISPLAY

(42) VCOM_DC Setting (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	-	VDCS[5:0]					

This command sets VCOM_DC value VDCS[5:0]: VCOM_DC Setting

VDCS[5:0]	Vcom value
00 0000b	-0.10 V
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(43) Partial Window (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Window	0	0	1	0	0	1	0	0	0	0
	0	1	HRST[7:3]					0	0	0
	0	1	HRED[7:3]					1	1	1
	0	1	-	-	-	-	-	-	-	VRST[8]
	0	1	VRST[7:0]							
	0	1	-	-	-	-	-	-	-	VRED[8]
	0	1	VRED[7:0]							
	0	1	-	-	-	-	-	-	-	PT_SCAN

This command sets partial window.

HRST[7:3]: Horizontal start channel bank. (value 00h~13h)

HRED[7:3]: Horizontal end channel bank. (value 00h~13h). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~127h)

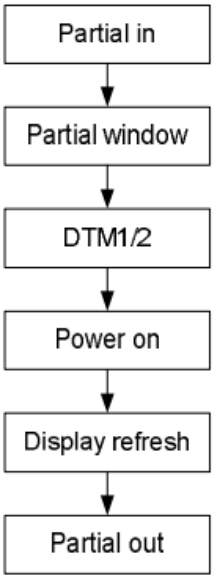
VRED[8:0]: Vertical end line. (value 000h~127h). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (default)

GOOD DISPLAY

Partial display flow:



(44) Partial In (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	0	1

This command makes the display enter partial mode.

(45) Partial Out (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial out	0	0	1	0	0	1	0	0	1	0

This command makes the display exit partial mode and enter normal mode.

(46) CRC Calculation in SRAM (CRCS) (R94H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
CRCS	0	0	1	0	0	1	0	1	0	0

Start to calculate data which already be sent to SRAM. The data are included OTP Bank 0 (3K bytes)or OTP Bank 1 (3K bytes) information

(47) CRC Calculation in OTP (CRCO) (R95H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
CRCO	0	0	1	0	0	1	0	1	0	1

The command define as follows: Start to Calculate data which already be programmed in OTP.

GOOD DISPLAY

(48) CRC status read (CRCR) (R96H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
CRCR	1	0	1	0	0	1	0	1	1	0
	1	0	CRC_MSB[7:0]							
	1	0	CRC_LSB[7:0]							

The command define as follows: This command is used to read the CRC calculation result.

(49) Write OTP key (OTP key) (R97H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
OTP key	0	0	1	0	0	1	0	1	1	0
	0	1	OTP key_MSB[7:0]							
	1	1	OTP key_LSB [7:0]							

The command define as follows: This command is used to unlock the OTP read function. The key must be same with the key (in 0xB76, 0xB77 OTP. And the OTP key could be decided by customer.

(50) Program Mode (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	1	0	1	0	0	0	0	0

After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.

(51) Active Program (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

After this command is transmitted, the programming state machine would be activated.

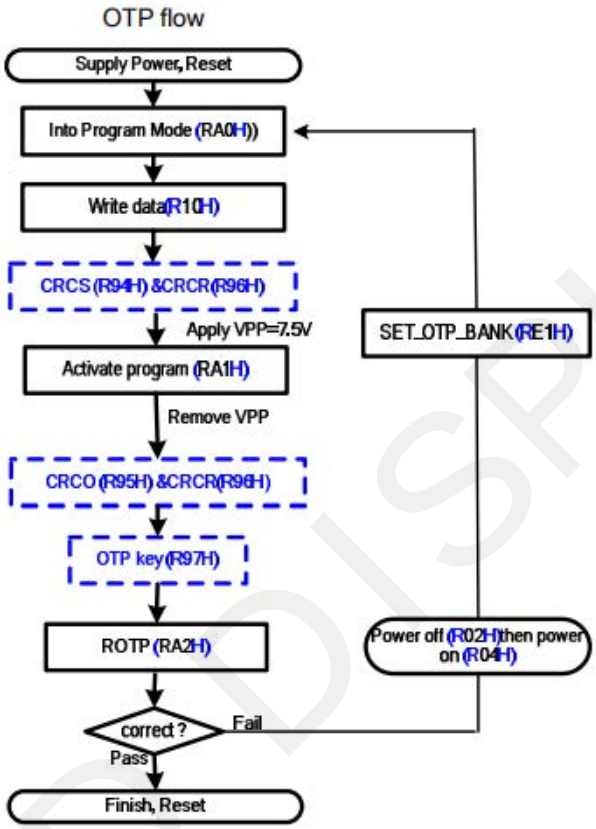
The BUSY flag would change state from 0 to 1 while the programming is completed.

(52) Read OTP Data (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP data for check	0	0	1	0	1	0	0	0	1	0
	1	1	Dummy							
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	..							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, tha max address = 0xFFF..



The sequence of programming OTP

(53) Cascade setting (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set cascade option	0	0	1	1	1	0	0	0	0	0
	0	1	-	-	-	-	-	-	TSFIX	CCEIN

This command is used for cascade.

CCEIN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

1: Temperature value is defined by TS_SET[7:0] registers.

(54) Set OTP program bank (SET_OTP_BANK) (RE1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set cascade option	0	0	1	1	1	0	0	0	0	1
	0	1	-	-	-	-	-	-	LUT_bank0	reg_bank0

This command is used to set program bank for registers and LUTs

OTP bank 0(3K Bytes)		OTP bank 1(3K Bytes)	
Address(Hex)	Content	Address(Hex)	Content
0x000~0x00B	Temp. segment	0xC00~0xC0B	Temp. segment
0x00C	Vcom DC voltage	0xC0C	Vcom DC voltage
0x00D~0xBFF	LUTs / Reserved	0xC0D~0x17FF	LUTs / Reserved

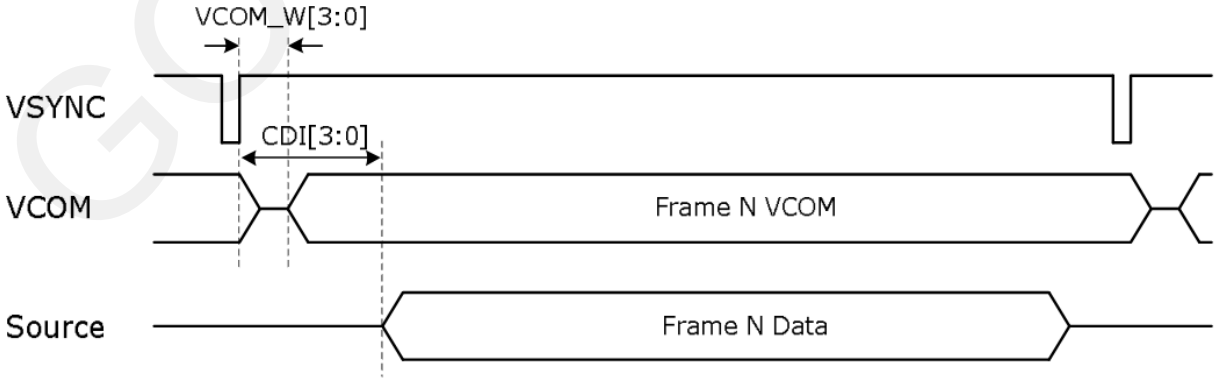
Bit	Name	Description
0	reg_bank0	0: Program “Temp. segment” and “Default Setting” in bank 1 1: Program “Temp. segment” and “Default Setting” in bank 0
1	LUT_bank0	0: Program “LUTs” in bank 1 1: Program “LUTs” in bank 0

After this command is transmitted, the programming state machine would be activated.

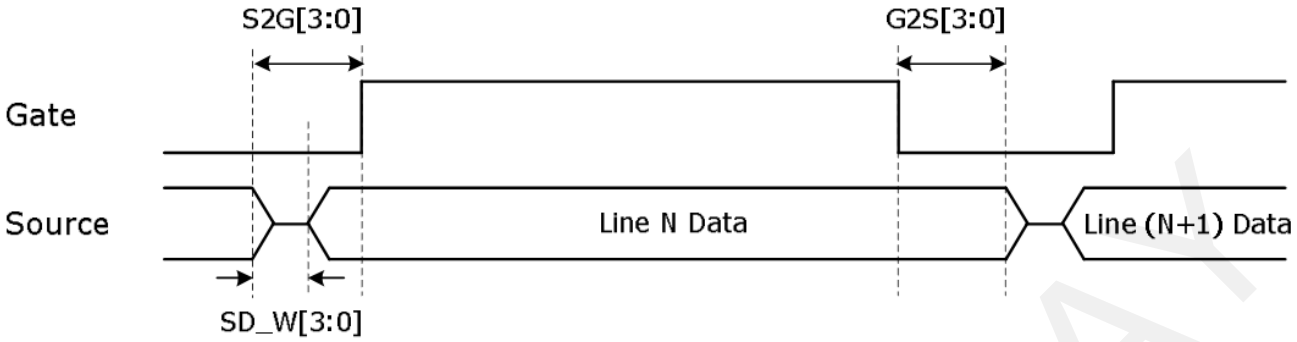
(55) Power Saving (PWS) (RE3H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Saving for Vcom &Source	0	0	1	1	1	0	0	0	1	1
	0	1	VCOM_W[3:0]				SD_W[3:0]			

This command is set for saving power during fresh period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters. VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



(56) LVD Voltage select (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Select LVD voltage	0	0	1	1	1	0	0	1	0	0
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]	

LVD_SEL[1:0]: Low Power Voltage selection.

LVD_SEL[1:0]	LVD value
00	＜2.2V
01	＜2.3V
10	＜2.4V
11	＜2.5V (default)

(57) Force Temperature (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Force Temperature value for cascade	0	0	1	1	1	0	0	1	0	1
	0	1	TS_SET[7:0]							

This command is used for cascade to fix the temperature value of master and slave chip in cascade.

GOOD DISPLAY

6. Optical characteristics

6.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 6-1
Gn	2Grey Level	-	-	DS＋(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	indoor	8	-	-	-	-
Panel's life		0℃~50℃		1000000 times or 5 years			Note 6-2

WS : White state, DS : Dark state

Gray state from Dark to White : DS、WS

m : 2

Note 6-1: Luminance meter : Eye – One Pro Spectrophotometer

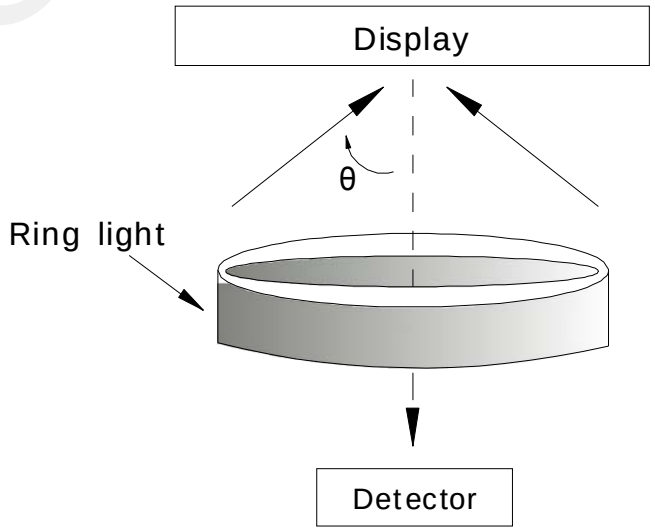
Note 6-2: Panel life will not guaranteed when work in temperature below 0 degree or above 50 degree. Each update interval time should be minimum at 180 seconds.

6.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd



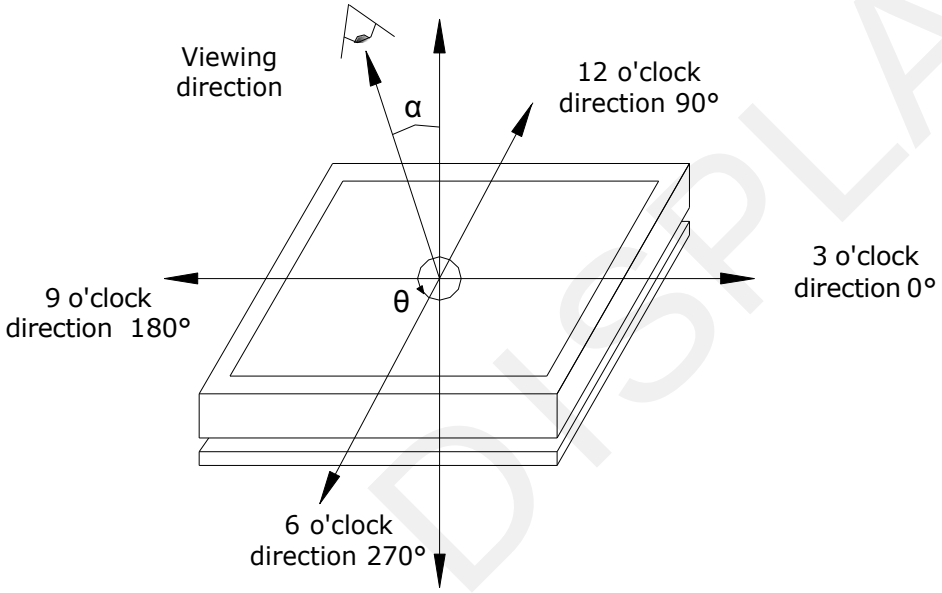
GOOD DISPLAY

6.3 Reflection Ratio

The reflection ratio is expressed as :

R = Reflectance Factor $_{white\ board}$ x (L_{center} / $L_{white\ board}$)

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{white\ board}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



6.4 Bi-stability

The Bi-stability standard as follows:

Bi-stability	Result		
		AVG	MAX
24 hours Luminance drift	White state △L*	-	3
	Black state △L*	-	3

GOOD DISPLAY

7. Point and line standard

Shipment Inseption Standard

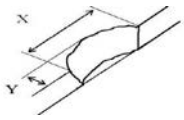
Part-A：Active area Part-B：Border area

Equipment：Electrical test fixture, Point gauge

Outline dimension：

31.8(H)*37.32(V)*0.98(D) Unit：mm

Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	23±2℃	55± 5%RH	1200～ 1500Lux	300 mm	35 Sec	

Name	Causes	Spot size		Part-A	Part-B
Spot	B/W spot in glass or protection sheet, foreign mat. Pin hole	D ≤ 0.15mm		Ignore	Ignore
		0.15mm < D ≤ 0.25mm		2	
		0.25mm < D		0	
Scratch or line defect	Scratch on glass or Scratch on FPL or Particle is Protection sheet.	Length	Width	Part-A	Ignore
		L ≤1.0mm	W≤0.1 mm	Ignore	
		1.0 mm<L≤2.5mm	0.1 mm<W≤0.2mm	2	
		2.5 mm < L	0.2mm < W	0	
Air bubble	Air bubble	D1, D2 ≤ 0.15 mm		Ignore	Ignore
		0.15 mm < D1,D2 ≤ 0.2mm		2	
		0.2mm < D1, D2		0	
Side Fragment					
	X≤3mm，Y≤0.5mm & display is ok, Ignore				

Remarks: Spot define: That only can be seen under WS or DS defects.

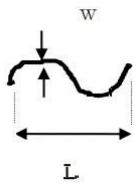
Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

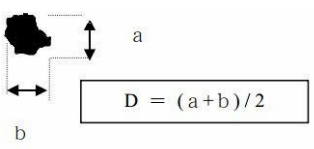
Here is definition of the “Spot” and “Scratch or line defect”.

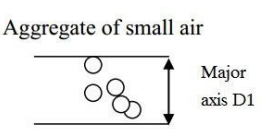
Spot: W > 1/4L Scratch or line defect: W ≤1/4L

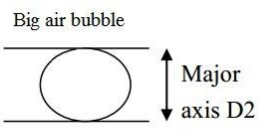
Definition for L/W and D (major axis)

FPC bonding area pad doesn’t allowed visual inspection.



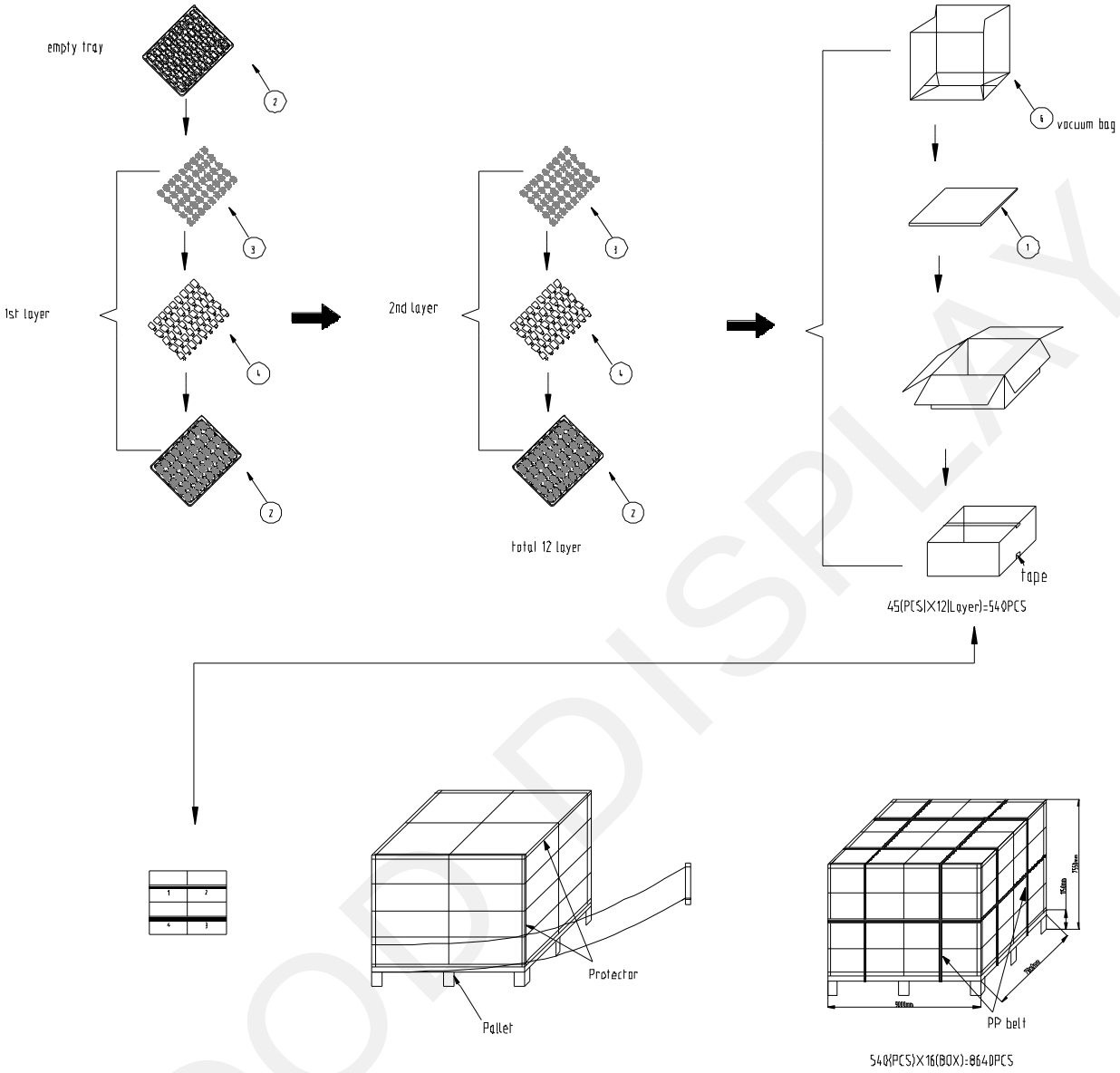






Note: AQL = 0.4

8. Packing



GOODDISPLAY

9. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

(7) For more precautions, please click on the link:
http://www.good-display.com/news/Precautions-for-E-paper-Display-80.html

GOOD DISPLAY